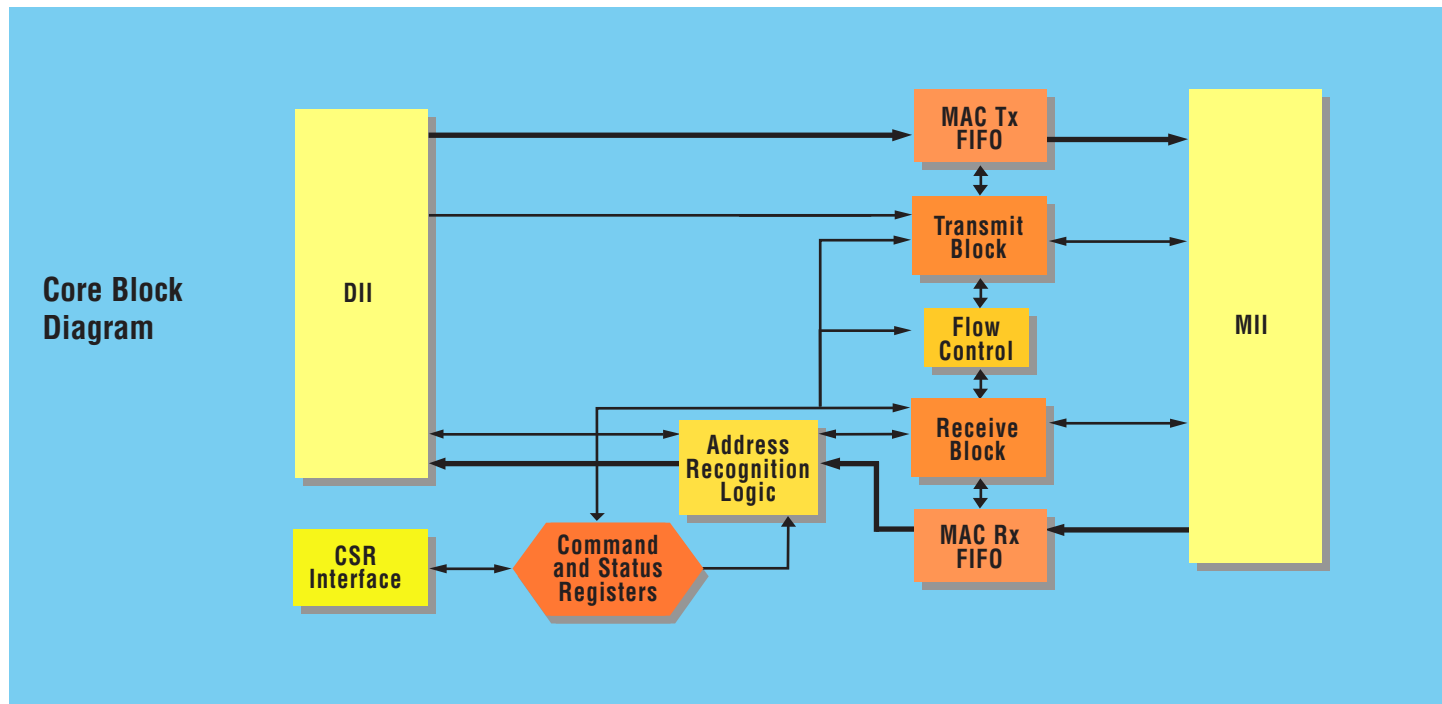


10/100 Mbps Ethernet MAC Core



► Features

- DMA Independent Interface (DII) for generic interface to the System Bus
- 10/100 Mbps Media Independent Interface (MII) for connecting various types of Physical Layers
- Optional 7-wire interface for connecting legacy 10 Mbps Physical Layer
- Full IEEE 802.3/802.3u compliant
- Address Recognition Logic (ARL) for destination address lookup and filtering
- Optional external CAM, ROM, or EEPROM interface
- PAUSE Flow Control operation for full-duplex link (802.3x)
- Parallel CRC and pad generation
- Command and Status Registers (CSR) that provide various soft-programmable features and minimize connection wires

► Benefits

- Soft core that can be implemented in any technology
- University of New Hampshire (UNH) compliant core
- IEEE 802.3/802.3u compliant core with PAUSE capability
- Optional serial interface for external ROM/EEPROM
- Synchronous Clock design
- Internal Scan and JTAG Boundary Scan that can be inserted by the customer before netlist handoff or by Fujitsu after design handoff

10/100 Mbps Ethernet MAC Core

► Description

The 10/100 MAC core is part of the Fujitsu IPWare™ Library. The 10/100 MAC core is a PAUSE Flow Control Ethernet Media Access Controller (MAC) capable of both 10 and 100 Mbps data operation. It is fully compliant with the IEEE 802.3 and 802.3u Specifications that employ Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. The PAUSE Flow control provides hardware support for full-duplex flow control.

The MAC has a standard MII for connecting to any 10 or 100 Mbps MII-supported PHY, such as 100Base-T4, 100Base-FX, 10Base-T, and 10Base-F. If the optional 7-wire interface is chosen, it can provide connection to the legacy 10 Mbps Physical Layer, namely 10Base-T, 10Base-2, 10Base-5, and even 10Base-F.

The DMA independent interface (DII) is a generic interface that uses a simple handshake protocol. It can be connected to a number of standard DMA interfaces and system buses, such as PCI, ISA, EISA, 680x0, nuBus, etc.

The CSR in the MAC ASIC core provides various soft-programmable features. These on-board registers also minimize the number of connection wires between the Bus Interface Unit and the MAC ASIC core. The CSR registers can be programmed to handle non-standard packet sizes such as Long Packets and Short Packets. Short Packets are very useful for fast testing.

► Deliverables

Fujitsu's application engineer works with customers and helps them select process technology that will suit the customer's specific need. After the technology is selected, the following can be supplied to the customer:

- Encrypted RTL source codes written in Verilog HDL representing the entire hierarchical MAC core design
- Encrypted Verilog Test Bench of the standalone MAC cores for functional verification
- A hierarchical gate level netlist of the MAC core

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