

Ultra-High-Speed CMOS Interface Technology

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Enhancing the performance of the broadband Internet and the performance of computer and storage systems requires high-bandwidth networks to interconnect these systems. Fujitsu has already marketed high-speed network interface products such as the 10G Ethernet and has recently developed a CMOS interface that accommodates high-speed data transfer at 6.4 Gb/s per signal line to increase network bandwidth. For this interface, we have developed a multi-tap pre-emphasis function for the transmitter and an adaptive equalizer for the receiver that can compensate for a high-frequency transmission loss of 20 dB or more in the backplane of devices and in cables that interconnect cabinets. When this CMOS interface is mounted on a system-on-a-chip (SoC) as a multi-channel interface, the system bandwidth can be upgraded significantly. This paper describes an ultra-high-speed CMOS interface that was manufactured experimentally using Fujitsu's 0.11 μm CMOS process.

1. Introduction

The demand for wide-bandwidth networks is increasing because of the rapid growth of broadband Internet access and the performance of computer and storage systems. A wider bandwidth network has also been required in home electronics appliances such as digital AV equipment to transfer large-volume image streams. This increase in speed is much higher than the speed increase that corresponds to the famous Moore's law prediction of LSI growth. The way to meet the wide-bandwidth network requirement and then improve performance through low power and low cost is to develop a high-speed CMOS interface and implement it in a system-on-a-chip (SoC). Fujitsu has already marketed high-speed network interface products such as multi-gigabit serial interfaces¹⁾ and is developing an ultra-high-speed serial interface that is as fast as 10 Gb/s.^{2),3)}

In addition, wide-bandwidth data transfer over long transmission traces such as backplane

connections in a cabinet and cable connections between cabinets are required to realize high-performance systems and appliances as well as higher speed transmission. Increases in the transmission speed and trace length of transmission lines increases the high-frequency loss and the associated Inter Symbol Interference (ISI). An ISI compensation scheme is required to achieve reliable data transmission in systems and appliances that have long trace transmission lines.

In response to the above, we have developed a high-frequency loss-compensation scheme that employs a multi-tap pre-emphasis filter for transmitter outputs and an adaptive equalizer for receiver front-ends. This scheme can compensate for losses of 20 dB or more in the backplane and/or cable connections. This paper describes a 12-channel, 6.4 Gb/s ultra-high-speed CMOS interface that implements this scheme and was manufactured using Fujitsu's 0.11 μm CMOS process.⁴⁾

2. Interface architecture

Figure 1 shows the 12-channel transceiver interface. Each channel in the transmitter interface multiplexes incoming 32-bit parallel data and outputs a 6.4 Gb/s differential serial data stream. Each channel in the receiver interface receives a 6.4 Gb/s serial data stream and demultiplexes it to 32-bit parallel data. The phase lock loop (PLL) supplies a high-frequency clock to each channel. Because the clocks for each channel are fed from a single PLL, the power dissipation and total area required are lower than in transceivers having a PLL for each channel.

2.1 PLL

We developed an LC tank type voltage-controlled oscillator (VCO) and applied it to the PLL of the interface to generate a high-frequency, low-jitter clock.^{2),3)} The LC tank circuit consists of an on-chip inductor (L) and on-chip variable capacitor (C). The PLL generates a high-frequency 3.2 GHz clock whose peak-to-peak jitter is less than 20 ps. Generally, an LC tank VCO's oscillation range is quite narrow due to the limited range of the variable capacitor. However, we achieved a wide frequency range of 2.5 to 3.2 GHz for all fabrication processes, operation temperatures, and supply voltage variations by developing a coarse and fine clock frequency adjustment circuit. The coarse adjustment is done by apply-

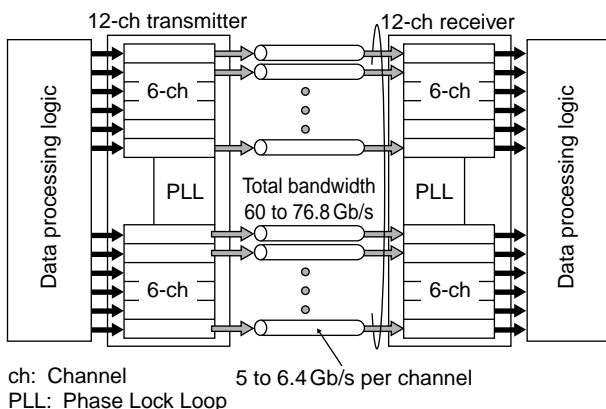


Figure 1
5 to 6.4 Gb/s 12-channel transceiver.

ing different variable capacitor voltages using an external digital control code. The fine adjustment is done by controlling the variable capacitor voltage in normal PLL frequency-lock operation.

2.2 Transmitter channel

Each transmitter channel consists of a 32:8 multiplexer (MUX), five 8:1 MUXs, and an output stage (**Figure 2**). The output stage includes five sets of drivers for a 5-tap pre-emphasis filter. Incoming 200 Mb/s, 32-bit parallel data is re-timed by the PLL clock and multiplexed to 800 Mb/s, 8-bit parallel data. Each 8:1 MUX drives one tap of the 5-tap pre-emphasis filter, and the last stage operates at 3.2 GHz, which is the half rate of the baud frequency. In the output buffer, the weight of each tap and the amplitude are controlled by external control signals.

2.3 Receiver channel

Each receiver channel consists of an equalizer, decision latch, 2:32 demultiplexer (DeMUX), clock recovery unit (CRU), and equalizer control circuit (**Figure 3**). Incoming 6.4 Gb/s serial data is received at the decision latch via the equalizer and demultiplexed into 200 Mb/s, 32-bit parallel data. The CRU uses a dual-loop PLL scheme consisting of an analog PLL and a digital PLL.²⁾ This scheme performs low power consumption clock data recovery (CDR) to enable bit-to-bit data skew adjustments and compensation for frequency variation between the transmitter and receiver clocks.

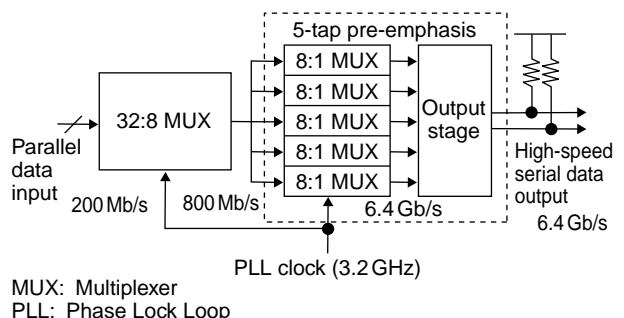


Figure 2
Transmitter channel.

The CRU monitors the bit cell boundary and the eye center, extracts the incoming data phase, and generates an incoming serial data sampling clock with the appropriate phase.

3. Transmission loss compensation

As the data rate increases in high-speed serial transmission, the skin effect in the metal conductors and dielectric loss in the insulators of transmission lines such as backplanes and cables increases and the ISI also increases. High-frequency loss on a 1 m backplane is estimated to exceed 20 dB at 3.2 GHz (6.4 Gb/s Nyquist frequency). The ISI strongly degrades waveforms at the receiver input and can prevent stable data communications. Therefore, the 6.4 Gb/s interface has two ISI compensation schemes: a 5-tap finite impulse response (FIR) filter circuit using pre-emphasis at the output stage of the transmitter channel and a second-order linear equalizer with adaptive control at the input stage of the receiver channel. These schemes emphasize the high-frequency component of the transmitted waveform that is degraded by the ISI. The high-frequency loss depends on the temperature as well as the trace length of the transmission line

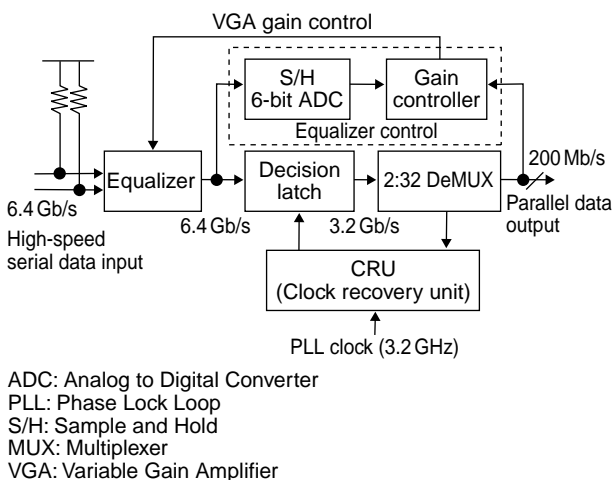


Figure 3 Receiver channel.

because the dielectric loss increases with temperature. The 5-tap FIR filter is controlled by preset parameters and compensates for backplane and/or cables losses. The equalizing parameters are dynamically adjusted using adaptive control to compensate for both static and dynamic losses. This scheme achieves a more than 20 dB loss compensation by controlling the compensation parameters according to the transmission system and its operation conditions. As a result, it enables reliable data communication at 6.4 Gb/s in backplane and/or cable connections.

3.1 Transmitter with pre-emphasis filter

The transmitter output stage consists of five blocks of differential drivers forming a 5-tap pre-emphasis filter (**Figure 4**). The delay per tap is 1 UI (Unit Interval), and a dedicated 8:1 MUX generates an appropriately delayed signal that drives each tap. The output voltage is pre-emphasized with a 1 UI width at 0-to-1 or 1-to-0 data transitions so the high-frequency component of the output waveform is increased in amplitude. The tap weights of the pre-emphasis filter are controlled via gates A1 to A5 of the current sources, and the output amplitude is controlled via gate B. The linearity of the tap weights versus the control voltage was improved by using a cascaded current mirror scheme in which the sources of the current mirrors for each tap are connected to a single shared current source. This scheme

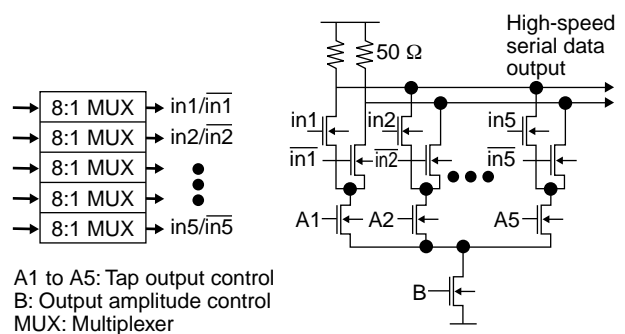


Figure 4 5-tap pre-emphasis filter.

provides good linearity for tap weight control and achieves output voltage control of the 5-tap amplifier within 5 mV, even though the transistors in the five amplifiers have different characteristics. The pre-emphasis filter can compensate for transmission losses of up to 20 dB in a 6.4 Gb/s data transmission.

3.2 Second-order equalizer

The receiver equalizer is a second-order high-pass filter composed of three pre-filters followed by variable gain amplifiers (VGAs) and an analog mixer (Figure 5). It has a 6-bit gain controller for each VGA. The transfer function of each pre-filter (Figure 6) is approximated to be 1 (flat), s (first derivative), and s^2 (second derivative) for frequencies below 3.2 GHz. The linear combiner sums the outputs of the VGAs, resulting in the following transfer function:

$$G(s) = as^2 + bs + c, \tag{1}$$

where a , b , and c are the VGA gains of the three paths controlled by the 6-bit controllers. The DC path sets the lower frequency component. The first and second derivative paths boost the gain

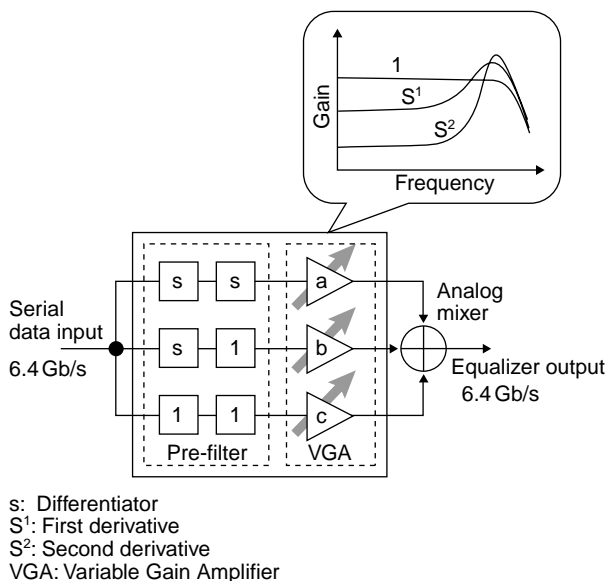


Figure 5 Equalizer with second-order high-pass filter.

for the higher frequency component and compensate for the high-frequency component of the transmitted waveform that is degraded by the ISI. The equalizer can compensate for transmission losses of up to 20 dB in a 6.4 Gb/s data transmission.

3.3 Adaptive control

To achieve the appropriate compensation for varying transmission losses, a variety of techniques that adaptively control the equalization strength have been reported.^{5),6)} In these reports, adaptive equalization control has been implemented using various analog circuits in both 5 Gb/s and 3.5 Gb/s CMOS transceivers. However, it is not easy to achieve a stable and programmable adaptation using analog controllers, which are affected by supply voltage, process, and temperature variations. Analog controllers also require a large capacitor area to achieve an appropriate time constant in the control loop. To address these issues, we developed a combined analog-digital adaptive equalizer controller (Figure 7). This controller consists of a sample and hold (S/H) circuit, 6-bit analog to digital converter (ADC), and VAG gain control logic. The S/H circuit samples the equalizer output voltage at 50 MHz, which is 1/128 of the baud rate. The sampled analog voltage is digitized by a 6-bit pipeline ADC. The appropriate VGA gain parameters to compensate for transmission losses are calculated by the gain control logic by monitoring the equalizer and decision latch outputs. The value of Ad_k , where A

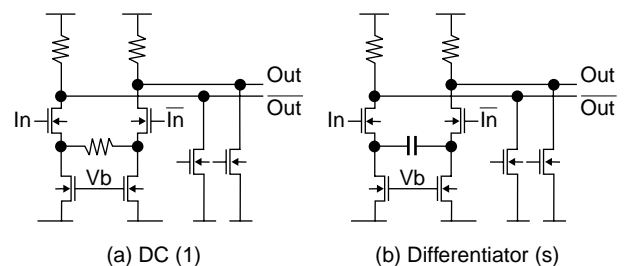
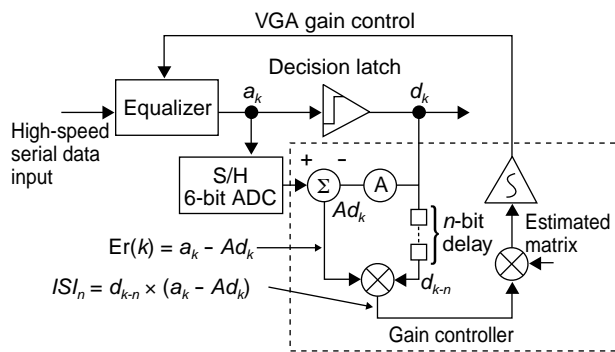


Figure 6 Pre-filter circuits.

is the desired signal amplitude and d_k is the digital value (either -1 or 1) of the received signal, is subtracted from the digitized equalizer output. This produces error signal $Er(k)$, which is the difference between the equalizer output a_k and ideal input Ad_k . The cross correlations between $Er(k)$ and d_{k-n} which is an n -bit delayed version of d_k , are calculated and fed back to the gains of each tap after multiplying a matrix and performing an integration.⁷⁾ This loop is settled so that $Er(k)$ becomes 0, resulting in an adaptive optimization of the equalizer parameters. A digital implementation of the algorithm requires 8000 gates and an area of around $150\ \mu\text{m} \times 300\ \mu\text{m}$.

4. Experimental results

Figure 8 shows photomicrographs of the 12-channel transmitter and receiver interfaces fabricated in Fujitsu's $0.11\ \mu\text{m}$ CMOS technology.



A: Desired signal amplitude
 ADC: Analog to Digital Converter
 S/H: Sample and Hold
 VGA: Variable Gain Amplifier
 ISI: Inter Symbol Interference

Figure 7
 VGA gain controller.

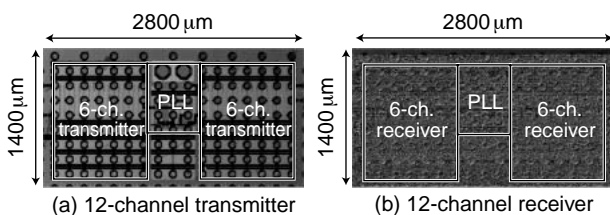


Figure 8
 Photomicrographs of 12-channel interfaces.

The area of each transmitter and receiver interface is $2800\ \mu\text{m} \times 1400\ \mu\text{m}$. The power consumptions of the 1-channel transmitter and receiver are 150mW and 90mW, respectively. The PLL consumes 90 mW.

Figures 9 (a) and 9 (b) show eye diagrams of a 6.4 Gb/s transmitter output without and with a pre-emphasis filter and with a 20 dB transmission loss. The eye opening cannot be observed without a pre-emphasis filter because of the 20 dB loss and the associated ISI. The pre-emphasis filter compensated for the ISI, and a clear eye opening was confirmed despite the 20 dB transmission loss. The single-ended eye opening voltage was larger than 100 mV. Figures 10 (a) and 10 (b) show eye diagrams of a 6.4 Gb/s receiver input at the equalizer output node without and with receiver equalization. The receiver input waveform was applied from the transmitter with a 20 dB loss and no pre-emphasis filter. The receiver equalizer removed much of the ISI degradation caused by the 20 dB loss, and a clear eye opening was confirmed. These results show it is possible to transmit a 6.4 Gb/s signal on

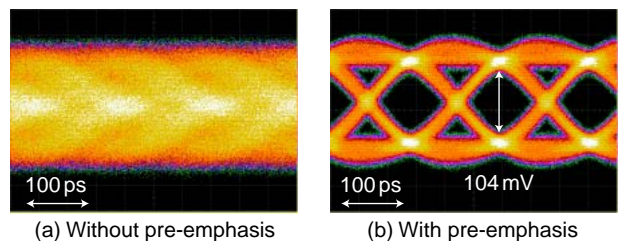


Figure 9
 Transmitter waveform after 20 dB loss.

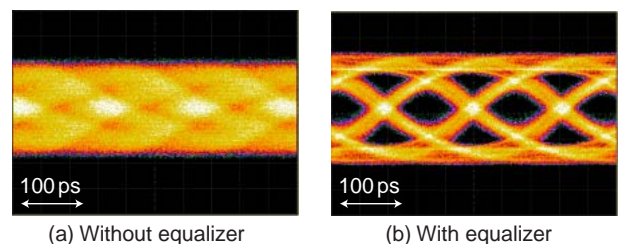


Figure 10
 Equalizer output waveform.

backplanes as long as 1 m by combining a pre-emphasis filter with receiver equalization. The measured bit error rate was confirmed to be less than 10^{-12} in loopback testing from the transmitter to the receiver interfaces with a 20 dB transmission loss.

5. Conclusion

A 6.4 Gb/s 12-channel parallel transceiver was developed using 0.11 μm CMOS technology. A 5-tap pre-emphasis filter and receiver equalizer with adaptive control achieved reliable 6.4 Gb/s data transmission with a more than 20dB transmission loss. This technology dramatically increases the bandwidth of backplane connections in a cabinet and cable connections between cabinets. It will enhance the performance of the broadband Internet and the performance of computers, storage systems, and home electronic appliances.



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