

This Customer Design Review Supplement is provided to prevent problems that may arise in the system development of MB91460P series. A complete system may not always be configured even if the following items are completely satisfied, but confirm at least the following items. We will recommend this Customer Design Review Supplement used to be filed as a review results.

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|------|---|--|---|----------|---|-----------|
| CPU | External reset | Does the reset input width satisfy the standards of Fujitsu? | If the reset input width does not satisfy the relevant standards, the CPU may not be able to return. | Yes / No | | 2008/3/25 |
| CPU | External reset IC | When external reset IC is used, are the low-voltage detection values within the operation guarantee range of the microcontroller? Do you take into account the voltage drop till generation after detection? | Malfunction may occur if a reset input is not within the operation guarantee range. | Yes / No | Check the operation guarantee range in the data sheet. | 2008/3/25 |
| CPU | Interrupt | Are interrupt vectors processed for undefined instruction exception interrupts ? | If an undefined instruction is executed such as by runaway, the runaway is accelerated. | Yes / No | When an undefined instruction is executed, a undefined instruction exception interrupt is caused. If a special type of processing is required, jump to the processing. If no special processing is required, it is recommended to jump to the reset vector. | 2008/3/25 |
| CPU | Interrupt | Are unused interrupt vectors processed? | If an unused interrupt is caused such as by runaway, the runaway is accelerated. | Yes / No | If a special type of processing is required, jump to the processing. If no special processing is required, it is recommended to jump to the reset vector. | 2008/3/25 |
| CPU | Bit operation instruction | In some resource registers, the use of the Read Modify Write instruction is prohibited. Do you use the Read Modify Write instruction in such registers? | Instruction execution may not normally be implemented and unexpected data may be written. | Yes / No | | 2008/3/25 |
| CPU | Main clock oscillation stabilization wait | Do you obtain the matching data of system and oscillator and know the required oscillation stabilization wait time? | There is fear that the CPU operates without normal oscillation. | Yes / No | Ask the vendor of the oscillator used for oscillation evaluation. | 2008/3/25 |
| CPU | Subclock oscillation stabilization wait | Do you perform a transition from the main mode to the subclock mode while subclock oscillation is still not stable? | The subclock requires longer oscillation stabilization time than the main clock. When the main clock mode changes to the subclock mode, therefore, subclock oscillation must be stabilized in advance. | Yes / No | Applicable only when the subclock is used. | 2008/3/25 |
| CPU | Clock | Do you switch to another mode during switching between internal clock operation modes (PLL, main,Sub)? | If you switch to another mode during switching between internal clock operation modes (PLL, main,Sub), a problem may occur at the switching timing. (It is prohibited to shift to the PLL mode during wait for stabilization of main clock oscillation.) *Single clock product doesn't be supported Sub mode. | Yes / No | See the relevant description in the manual. | 2008/3/25 |
| CPU | Clock | Is the oscillation stabilization wait time set when a transition occurs from the PLL mode directly to low power consumption mode such as the stop mode, not via the main mode? | The PLL clock mode can be changed directly to low power consumption mode such as the stop mode. In this case, however, the oscillation stabilization wait time in consideration of the PLL lock time needs to be set at return. | Yes / No | | 2008/3/25 |
| CPU | Clock | Are timebase timer interrupts prohibited during state transition from the main mode to the PLL mode or from the main mode to the submode? | The timebase timer is used to count the oscillation stabilization wait time and the PLL clock stabilization wait time. Therefore, the counter is automatically cleared when one of the following state transitions occurs: - Transition from main clock mode to PLL clock mode - Transition to subclock mode - Transition to stop mode Timebase timer interrupts must be prohibited during state transition from the main mode to the PLL mode or from the main mode to the submode. Otherwise, an unexpected timebase timer interrupt may occur. | Yes / No | | 2008/3/25 |

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| CPU | Transition to standby mode | Do you know precautions on the transition to standby mode? | To enter the standby mode with synchronous standby operation (TBCR.SYNCS = 1) enabled, the STCR register must be read once after writing to the relevant control bits (sleep and stop bits). (LDI #value_of_standby, R0) ; // STCR write data is included in value_of_standby. (LDI # STCR, R12) ; // .STCR is the STCR address (481H). STB R0, @R12 ; // Writes to the standby control register (STCR). LDUB @R12, R0 ; // STCR needs to be read for synchronous standby. LDUB @R12, R0 ; // Second dummy read of STCR NOP ; // Five NOPs are required to take timing. NOP NOP NOP | Yes / No | | 2008/3/25 |
| Peripheral function | I/O port | Is processing such as rewriting to important port I/O enabled for the purpose of fail safe in the system? | Basically, the status of a port does not change unless defined by software. For the purpose of fail safe in the system, however, it is recommended to insert a refresh function, implemented by software, such as for rewriting to important ports. | Yes / No | | 2008/3/25 |
| Peripheral function | I/O port | When the CMOS I/O port is used for output, is the PDRx register set first and then the DDRx register? (FR30 series) When the CMOS I/O port is used for output, are the PDRx, DDRx, and PFRx registers set sequentially in this order? (FR60 series) | Because the initial value of the PDRx register is undefined, undefined data is output if the DDRx register is set for output without setting the PDRx register. When the CMOS I/O port is used for output, set the PDRx register first and then set the PFRx register if used. | Yes / No | | 2008/3/25 |
| Peripheral function | ADC | Is analog input impedance below that specified in the data sheet? If the analog input impedance is higher, the sample hold time needs to be set longer or a capacitor needs to be attached externally. | If analog input impedance is higher, the analog data sampling time may become insufficient. | Yes / No | Applicable only when an A/D converter is used. | 2008/3/25 |
| Peripheral function | ADC | Is sufficient analog sample hold time secured? | If analog input impedance is high, a glitch may occur in the analog input pin. The glitch is caused depending on the analog input impedance as the time constant of the internal capacitance. If the sample hold time is shorter, the sample hold time may be affected by the glitch. (Because differences may also occur with Flash or Mask, sufficient sample hold time should be secured when analog input impedance is higher.) | Yes / No | Applicable only when the recommended analog input impedance in the data sheet or higher is used. | 2008/3/25 |
| Peripheral function | ADC | Do you finish A/D conversion and start A/D simultaneously? | If the end of A/D conversion and A/D startup occur simultaneously, the second start may be ignored. | Yes / No | Applicable only when A/D is started while A/D is in progress. | 2008/3/25 |
| Peripheral function | ADC | Are the (AVR or AVRH) and AVCC voltage levels sufficiently stable? | Reactance may be put in AVR and AVCC to perform power separation between the analog and digital power supplies. In this case, circuits should be configured to enable sufficient power supply at A/D converter startup such as by adding a capacitance of several uF or more to AVR and AVCC. | Yes / No | Applicable only when the A/D converter is used. | 2008/3/25 |
| Peripheral function | Flash | Do you know that flash memory cannot be read during writing to memory or deletion of memory data (chip deletion, sector deletion)? | Interrupt vectors in flash memory cannot be read either during writing to memory or deletion of memory data (chip deletion, sector deletion). Note that interrupt processing thus cannot be performed during writing or deletion. | Yes / No | Applicable only when user writes data in flash memory. | 2008/3/25 |
| Peripheral function | Flash | When flash memory user writing is supported, is flash writing controlled by using the hardware sequence flag? | Because the FSTR register cannot be used for write/delete error checking, Fujitsu recommends using the hardware sequence flag to implement flash write/delete control. | Yes / No | Applicable only when user writes data in flash memory. | 2008/3/25 |

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| Peripheral function | I2C | Is the AL bit checked after master mode setting (writing 1 to the MSS bit)? | If master mode is set (writing 1 to the MSS bit) while the SCL or SDA pin is Low, start condition generation and SCL clock output are disabled and a transfer end interrupt (INT bit) is not caused. Therefore, after master mode is set (writing 1 to the MSS bit), check the AL bit to detect this state after waiting for the 3-bit data transfer time. (It takes the 3-bit data transfer time after setting the MSS bit to 1 for the AL bit to change.) | Yes / No | Applicable only when I2C is used. | 2008/3/25 |
| Peripheral function | I2C | Is the operating frequency of this product type set in such a way that the data setup time standard of the communication destination is satisfied? | Set the operating frequency of this product type in such a way that the data setup time standard of the communication destination is satisfied | Yes / No | Applicable only when I2C is used. | 2008/3/25 |
| Peripheral function | I2C | Is the INT bit cleared at the end of interrupt routine processing? | In accordance with the specifications, the SCL pin goes low when INT bit is 1 and the SCL pin is open when the INT bit is cleared. Therefore, I2C data processing needs to be performed when INT bit = 1 (SCL pin = Low), and the INT bit needs to be cleared (making the SCL pin open) when transmission/reception of next data is enabled. | Yes / No | | 2008/3/25 |
| Peripheral function | I2C | When the I2C bus is used, are alternate pins set for input (DDR = 0)? | In the case where a Read Modify Write instruction may be executed for the same series (Px0 to Px7) of I2C bus alternate pins (Pxy/SCK0, Pxz/SOT0) while the alternate pins are set for output, the execution of the Read Modify Write instruction probably changes PDR (Pxy, Pxz). If the I2C bus is prohibited under this condition, the changed values of PDR (Pxy, Pxz) are output to ports. | Yes / No | Applicable only when I2C is used. | 2008/3/25 |
| Peripheral function | Hardware watchdog timer | Is the hardware watchdog timer cleared regularly? (HWDCS: CL bit) | The hardware watchdog timer immediately starts its operation after the release of resetting. Software cannot stop counting. A reset signal is generated unless the timer is cleared regularly by software. | Yes / No | Before transition to a mode in which the CPU does not run (SLEEP, STOP, SHUTDOWN, or RTC mode), the timer is cleared and counting is stopped. Also, while the debug routine is running via DSU, the watchdog timer is cleared and counting is stopped. However, a reset is issued if the DMA transfer time is longer than the watchdog period. | 2008/3/25 |
| Peripheral function | Watchdog timer | Is the watchdog timer cleared by a timer interrupt? | If watchdog reset intervals are not sufficiently specified, it is difficult to detect whether the program runs according to normal procedures. | Yes / No | | 2008/3/25 |
| CAN related item | Reception error and bus-off | Do you know there is no possibility of a bus-off by the reception error? | In the software development, a countermeasure against a bus-off due to a reception error is invalid. | Yes / No | | 2008/8/8 |
| CAN related item | High-speed CAN and oscillator accuracy | For a high-speed CAN data communication, is the highly accurate oscillator used? | As the allowable error of the oscillator depends on the baud rate of CAN, the large error of the oscillator may prevent the normal communication. | Yes / No | | 2008/8/8 |
| CAN related item | CAN baud rate | Do you make the settings that consider the condition of each segment to decide the CAN baud rate? | There is a possibility that the CAN transmission and reception are not executed normally. | Yes / No | Confirm whether the requirement of TSEG1 '2TQ, TSEG1 ' RSJW, TSEG2 ' 2TQ, and TSEG2 ' RSJW in the manual is met. | 2008/8/8 |
| CAN related item | IDR | Is the message buffer (BVAL) enabled without setting ID in ID? | An initial value of IDR that sets ID is indefinite. Therefore, there is a possibility of receiving the indefinite data of ID when the target message buffer is enabled though the value is not set. | Yes / No | | 2008/8/8 |
| CAN related item | Regarding with DIR | Mdir bit should not be masked. | In hardware manual, it said Mdir bit should not be masked . | Yes / No | Please refer to hardware manual. | 2008/8/8 |
| CAN related item | A restriction on C_CAN | Do you have been informed about the restriction on C_CAN macro? | The related report has been published individually, please contact with our sales. | Yes / No | | 2008/8/8 |
| General | General | In linker layout/linkage, is the memory range set according to the ROM and RAM amounts of the Flash and Mask products? | The internal memory amount of the EVA chip for evaluation differs from those of the Flash and Mask products. For this reason, even if normal operation can be confirmed with the tool, operation may be disabled on the actual products. | Yes / No | | 2008/3/25 |

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| General | General | Is the maximum usage of the stack checked? | Incorrect estimation of stack usage may result in damage to RAM. | Yes / No | The maximum usage of the stack should be checked using the Softune C analyzer. (Because the C analyzer cannot check dynamic stacks, it is necessary to check the maximum usage in consideration of the occurrence of concurrent multiple interrupts.) | 2008/3/25 |
| General | General | Do you issue a Read Modify Write instruction in a register that includes a write-only bit? | If a Read Modify Write instruction (such as BANDL) is used in a register that includes a write-only bit, an undefined value is read from the write-only bit and a problem may result. (This problem does not occur with the registers for which the manual describes, the use of Read Modify Write instructions causes no problem.) | Yes / No | For development with a C source, check whether a header file is used to set a RMW instruction in bit units in a register that includes a write-only bit. The Read Modify Write (RMW) instructions mean those for which * is marked for RMW in the instruction list | 2008/3/25 |
| General | General | Do the voltage range used, temperature range used, and operating frequency used satisfy the Fujitsu-specified standards? If not, do you consider or have any agreement for special guarantee? | Product guarantee is not available when the product is used out of the guarantee range. | Yes / No | Check the operation guarantee range in the data sheet. | 2008/3/25 |
| Noise countermeasures and others | Mode pin | Is the same level secured for MOD pin processing even during instruction execution? | There is fear that the MOD pin level is read incorrectly. (When the MOD pin is processed by a high impedance resistor, the MOD pin level may not be secured due to noise.) | Yes / No | If external noise is likely to intrude into the MOD pin, countermeasures against static electricity such as connecting a capacitor to the mode pin should be taken. | 2008/3/25 |
| Noise countermeasures and others | Mode pin | Is the MOD pin processing interconnect moderately short (not too long) and free from large current signals in the neighborhood? | There is fear that the MOD pin level may be read incorrectly due to power fluctuation or noise. | Yes / No | | 2008/3/25 |
| Noise countermeasures and others | Oscillation | When a crystal oscillator is used, is an adequate dumping resistor inserted? | When a crystal oscillator is used, a dumping resistor is required for suppressing oscillation current. | Yes / No | Ask the vendor of the oscillator used for oscillation evaluation. | 2008/3/25 |
| Noise countermeasures and others | Oscillation | Do you collect oscillation matching data with mass-produced products? | Oscillation characteristics may differ between flash and mask products. It is recommended to collect oscillation matching data with mass-produced products. | Yes / No | Ask the vendor of the oscillator used for oscillation evaluation. | 2008/3/25 |
| Noise countermeasures and others | Oscillation | Are unnecessary radiant noise and oscillation amplitude recognized to determine the dumping resistance of the oscillating circuit? | Oscillation may not normally be performed, or unnecessary radiant noise may increase due to oscillation overshoot or undershoot. | Yes / No | If a problem of unnecessary radiant noise occurs, it is needed to study inserting a dumping resistor as measures against unnecessary radiant noise while confirming oscillation waveforms. | 2008/3/25 |
| Noise countermeasures and others | Oscillation | Is the oscillator placed as close to the chip as possible? | The CPU may cause a runaway due to external noise. | Yes / No | Be sure to place the oscillator near chips. | 2008/3/25 |
| Noise countermeasures and others | Vcc,GND | Is it designed to make Vcc and GND as resistant to noise as possible? | There is fear of unnecessary-radiant noise problems and the CPU running into out of control due to external noise. | Yes / No | Consider preventing unnecessary radiant noise and external noise in advance, and secure the power and GND areas as wide as possible. (Placing GND under chips can enhance GND.) | 2008/3/25 |
| Noise countermeasures and others | ESD, latch-up, noise | Are ESD, latch-up, and noise evaluations performed with mass-produced products? | Because ESD, latch-up, and noise performance differ between flash and mask products, it is recommended to evaluate such performance with mass-produced products. | Yes / No | For performance data with mask and flash products, Fujitsu is ready to submit internal measurement results as performance examples upon request. | 2008/3/25 |
| Noise countermeasures and others | Capacitor | Is a most appropriate capacitor connected near the product for countermeasures against noise? | The capacitor placed for measures against noise may be impaired by reactance components of lead lines. (Countermeasures with noise components taken into account are needed.) | Yes / No | | 2008/3/25 |

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| Noise countermeasures and others | Unused-pin processing | Is an unused pin pulled up or down with a 2kΩ or higher resistor? Or, is port output processing performed in the initial routine while the pin is left open? | If an unused pin is processed without intervention of a resistor, a problem such as latch up may occur if the port level output is opposite to the processing level due to CPU runaway. | Yes / No | | |
| Noise countermeasures and others | Special guarantee | You may have a contract of special guarantee. If so, did you return the paper with "confirmation stamp (problem: yes/no)" clearly stated to your salesperson? | If you have a contract of special guarantee, a test change may be needed. Be sure to return the paper before the ROM release. | Yes / No | Because it may take a few months to respond to a test change, it may be too late to respond if you return the paper immediately before the ROM release. | 2008/3/25 |
| | | | | | | 2008/3/25 |