This check sheet is provided to prevent problems that may arise in the system development of MB90580series.
A complete system may not always be configured even if the following items are completely satisfied, but confirm at least the following items.

Item		Content	Reason	Result	Remarks
CPU	Power-on reset	Is the standard on electrical characteristics concerning power-on reset being met?	Powering on without meeting the power-on reset standard may result in the execution of commands by CPU without the power-on reset implemented normally.	Yes / No	Applied to systems using reset at power-on (Not applied to systems using power monitoring IC for reset equivalent input).
		Are you aware of the registers (CKSCR, LPMCR) that are initialized only by power-on reset?	The registers that are initialized only by power-on reset (CKSCR, LPMCR) are very important registers. In cases where, in terms of system operations, power-on reset cannot be implemented, we recommend using the system by taking the following step described in the manual: HSTX+RSTX (shorting HSTX and RSTX).	Yes / No	
	External reset	Does the reset range meet the Fujitsu's standard?	When the reset range does not meet the Fujitsu's standard, recovery cannot be implemented.	Yes / No	
	Reset cause bits	When using the watchdog timer control (WDTC) register's reset cause bits, is the WDTC register read once by using the program default setting, followed by the clearing of the reset cause bits?	The default values of all reset cause bits are undefined. Accordingly, in order to clear all reset cause bits, ensure that the WDTC register is read once before using it.	Yes / No	Applied only when reset cause bits are used.
	PLL->Main	In software development, is attention given to the timing of the changes in the CPU's operation speed during the status transition of Main -> PLL -> Main -> PLL when such processing speed does change? (Is consideration given to the need to wait for eight cycles between MCS "1" write and "0" write?)	Within the eight cycles between MCS "1" write (Main) and "0" write (PLL), "0" write can be ignored.	Yes / No	Refer to the explanation of the MSC bit in the manual.
	Main(PLL) -> Sub -> Main(PLL)*	In CPU status transitions, during status transition of Main or PLL -> Sub -> Main or PLL, is it verified, prior to transition to another status, that the CPU is transferred to statuses set by using the MCM and SCM bits?	Between the "0" write (Sub) and the "1" write (Main) to SCS, "1" write can be ignored within one sub clock cycle. When switching SCS, modify SCS only after verifying that transition to the status expected in SCM occurs.	Yes / No	Refer to the explanation of the SCM bit in the manual.
	PLL -> Sub(Stop) -> PLL	For direct transition to PLL mode following the release of main clock stop status, is the oscillation stabilization wait time of the main clock set longer than the PLL clock wait time?	When transition to PLL mode recurs after transition from PLL mode to sub RUN (or STOP) status, the oscillation stabilization wait time of the main clock should be set longer than the PLL clock wait time.	Yes / No	
	Switching of the internal clock operation mode	When switching the internal clock operation mode (PLL, main, sub), is the operation mode switched to another mode?	If, when switching the internal clock operation mode (PLL, main, sub), the operation mode is switched to another mode, problems may arise when switching the mode (Behavior such as attempting to transition to the PLL mode during main clock oscillation stabilization wait time in transition from sub-clock oscillation to main clock oscillation is prohibited).	Yes / No	See the explanation of the MCS and SCM bits in the manual.
	Time-base timer	Do you know that the counter of the time-base timer is cleared automatically by hardware?	Since the time-base timer is used as a counter of the oscillation stabilization wait time and PLL clock stabilization wait time, the counter is automatically cleared in the following state transitions: - Transition from the main clock mode to the PLL clock mode - Transition to the subclock mode - Transition to the stop mode When the time-base timer interrupt is not prohibited during state transition from the main mode to the PLL mode or from the main mode to the sub-clock mode, an unintended time-base timer interrupt may occur.	Yes / No	
	A/D converter	Is analog impedance the analog impedance described in the datasheet or less. When the analog impedance is higher, it is required to set the sample hold time longer or install an external capacitor of approximate 0.1 uF.	When the analog impedance is higher, the sampling time of analog data may become shorter than required time.	Yes / No	Only when A/D converter is used.
		Is voltages of AVR and AVCC are sufficiently stable?	To separate power supplies of analog system and digital system, a reactance device may be mounted in AVR and AVCC. In this case, it is reconmmended to configure the circuit by adding a capacitor of some micro F so that sufficient power is supplied at A/D start.	Yes / No	Only when A/D converter is used.

This check sheet is provided to prevent problems that may arise in the system development of MB90580series.
A complete system may not always be configured even if the following items are completely satisfied, but confirm at least the following items.

Item		Content	Reason	Result	Remarks
		Is analog sampling time sufficiently long?	When anolog input impedance is larger, a glitch may occur at analog input pin.. The glitch is determine by the analog impedance and time constant of internal capacitance. When sample hold time is shorter, sample hold value may be affected by the glitch. Because the influence of the glitch is different beteween FLASH product and MASK product, it is recommmended to set a sufficient sample hold time when the analog input impedance is larger.	Yes / No	Only when the analog input impedance used is larger than the analog input impedance recommended by th Data Sheet.
		Are the completion and start of A/D conversion implemented at the same time?	When the comletion and start of A/D conversion are implemented at the same time, the later operation, the start of the A/D conversion, may be ignored.	Yes / No	Only when A/D conversion is started during A/D conversion performed.
		Is the analog input enable register(ADER) set to port input mode, when A/D converter is used?	When the port input mode is set with the ADER and A/D input (voltage of medium potential) is implemented, through current flows in CMOS input circuit of I/O port and the current consumption is increased.	Yes / No	Only when A/D converter is used.
	Unused pin treatment	Is any unused pin pulled up or pulled down by the resistor of 2 kΩ or more? Or, is the port output treatment performed in the initial routine by leaving the pin opened?	When an unused pin is treated without a resistor and the port level opposite to the processing level is output due to CPU runaway, problems such as latch-up may arise.	Yes / No	
	Interrupt	Is the interrupt vector processing of an exceptional interrupt performed?	Runaway may be caused when an undefined instruction is executed due, for example, to runaway.	Yes / No	When an undefined instruction is executed, an exceptional interrupt occurs. Thus, when special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended.
		Are interrupt factors cleared in the main routine?	Since interrupt factors may be cleared and set simultaneously, it is recommended to clear interrupt factors in an interrupt routine. When interrupt sources are to be cleared in the main routine, it is recommended to clear them after prohibiting interrupts of the target peripheral.	Yes / No	Since, particularly for UART, reception interrupts are set asynchronously, it is recommended to clear interrupt factors in an interrupt routine so that they should not occur simultaneously with reception interrupt setting or clear them after prohibiting reception interrupts.
		Is processing of an unused interrupt vector performed?	Runaway may be caused when an unused interrupt occurs due, for example, to runaway.	Yes / No	When special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended
	Bit manipulation instruction	Read-modify instruction is prohibited by some registers of each resource. Is any RMW instruction used in the target register?	The instruction may not be executed normally, resulting in unintended data being written.	Yes / No	Read-modify-write related instruction is indicated in the instruction list by * in RMW.
	Main clock oscillation stabilization wait	Is the required oscillation stabilization wait time identified by obtaining matching data of the system and oscillator?	CPU may be run before oscillation has stabilized.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.
	Subclock oscillation stabilization wait	Has the state transition from the main mode to the subclock mode taken place while the subclock oscillation is still unstable?	The subclock needs longer oscillation stabilization time than the main clock does. Thus, before the state transition to the subclock mode takes place, oscillation of the subclock needs to stabilize.	Yes / No	Only when the subclock is used
	Watchdog	Is the watchdog timer cleared by, for example, a timer interrupt? (Are incorrect PLL multiplication settings and the intermittent operation mode considered?)	When the watchdog reset interval is not sufficient, whether a program is proceeding normally cannot be detected.	Yes / No	
		When using the built-in watchdog timer during sub-clock operation, is the watchdog clock resource set so that the clock timer is used (WDCS=0)?	When using the built-in watchdog timer during sub-clock operation, if the time-base timer is set as the watchdog clock resource (WDCS=1), no watchdog may be generated during sub-clock operation.	Yes / No	
	External reset IC	When using external reset IC, is the low-voltage detecting value within the guaranteed operation voltages of the microcomputer? Is the voltage drop between detection and reset considered?	When no reset within the guaranteed operation voltages is entered, a malfunction may occur.	Yes / No	Confirm the guaranteed operation voltage range in the data sheet.
	I/O port	Do you know that, after power-on, the output level of port is undefined during clock oscillation stabilization wait time?	For more details of the target port, see "Device handling" in the hardware manual and data sheet.	Yes / No	Only when the RSTX pin is "H" during power-on reset

This check sheet is provided to prevent problems that may arise in the system development of MB90580series.
A complete system may not always be configured even if the following items are completely satisfied, but confirm at least the following items.

Item		Content	Reason	Result	Remarks
		Is processing such as additional writing performed for the purpose of a fail-safe system in important port input/output?	Basically, the port state does not change as long as not set by software. However, for the purpose of making the system fail-safe, it is recommended to insert software of a refresh function such as additional writing into important ports.	Yes / No	
		When using the CMOS I/O port for output, is the DDRx register set after setting the PDRx register?	Since the initial value of the PDRx register is undefined, if the DDRx register is set for output without setting the PDRx register, the output becomes undefined. Before setting the DDRx register for output, set the PDRx register first.	Yes / No	
	Flash	Do you know that FLASH memory cannot be read while writing to/deleting (chip deletion/sector deletion) FLASH memory?	While writing to/deleting (chip deletion/sector deletion) FLASH memory, no interrupt vector on FLASH memory cannot be read, either. Thus, remember that no interrupt processing can be performed while writing/deleting.	Yes / No	Only when FLASH memory is written by the user
		When users are allowed to write to FLASH memory in user programming mode, is the hardware sequence flag used to control writing to FLASH memory?	Since the FMCS register cannot be used to check for write/delete errors, it is recommended to use the hardware sequence flag to control writing to/deleting FLASH memory.	Yes / No	Only when FLASH memory is written to by the user
	General	Do the voltage, ambient temperature, and operating frequency ranges satisfy the standards specified by Fujitsu? When any of them does not satisfy the standards, is any special guarantee considered and supported?	When not used within the guarantee range, no product guarantee can be provided.	Yes / No	Check the guaranteed operation range in the data sheet.
		When a special guarantee is considered, is a notification form returned to the Sales Dept. after affixing a "confirmation stamp ((No problem, Problem found) in the reply)" on the notification form?	If a special guarantee is provided, test changes may be needed. Thus, make sure to return the notification form before ROM release.	Yes / No	Since it may take up to several months to deal with test changes, they may not be dealt with when the notification form is returned just before ROM release.
Noise reduction measures and others	Mode(MOD) pin	Is the same level for processing of the MOD pin ensured even while executing instructions?	The level of the MOD pin may be read incorrectly (When a high-impedance resistor is used for treating the MOD pin, the MOD pin level may not be ensured due to noise).	Yes / No	When external noise tends to propagate to the MOD pin, it is recommended to take countermeasures against static electricity such as connecting a capacitor to the mode pin.
		Is interconnect for treating the MOD pin too long or is there any adjacent high current signal interconnect?	The level of the MOD pin may be read incorrectly due to power supply deviation and noise.	Yes / No	
	Oscillation	When using a crystal oscillator, is an appropriate dumping resistor inserted?	To use a crystal oscillator, a dumping resistor to reduce the excitation current is needed.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.
		Is oscillation matching data of mass-produced products obtained?	Since oscillation characteristics of flash products and those of mask products may be different, it is recommended to obtain oscillation matching data of mass-produced products.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.
		Is the resistance of the dumping resistor for the oscillation circuit determined in view of unnecessary radiation noise and oscillation amplitude?	When oscillation is abnormal or an overshoot or undershoot of oscillation occurs, unnecessary radiation noise may increase.	Yes / No	When a problem of unnecessary radiation noise arises, it is necessary to first confirm the oscillation waveforms and then examine whether to insert a dumping resistor as a measure to reduce unnecessary radiation noise.
		Is the oscillator arranged as close to the chip as possible?	CPU runaway due to external noise may be presumed.	Yes / No	It is recommended to arrange the oscillator as close to the chip as possible?
	Vcc, GND	Is consideration given to making Vcc and GND as strong as possible?	Problems of unnecessary radiation noise and CPU runaway due to external noise may be presumed.	Yes / No	To avoid problems of unnecessary radiation noise and external noise, it is recommended to take the power supply and GND as widely as possible (By arranging GND under the chip, for example, the GND can be strengthened).

This check sheet is provided to prevent problems that may arise in the system development of MB90580series.
A complete system may not always be configured even if the following items are completely satisfied, but confirm at least the following items.

Item		Content	Reason	Result	Remarks
	ESD, latch-up, noise	Are mass-produced chips used to evaluate ESD, latch-up, and noise resistances?	Since the resistances against ESD, latch-up, and noise of Flash products and those of mask products are different, it is recommended to use mass-produced products to evaluate ESD and latch-up resistance.	Yes / No	Since it is possible to submit measurement results of Fujitsu as characteristic examples of resistance characteristic data between MASK and FLASH products, make a request of them.
	Capacitor	Is the optimum capacitor connected near the chips as a capacitor for reducing noise?	The capacitor connected to reduce noise may not work with reactance components of interconnect (Measures that take noise components into account are needed).	Yes / No	
	C pin	The capacitance of the smoothing capacitor connected to Vcc is larger than that of the capacitor connected to C pin?	When the capacitance of the smoothing capacitor is smaller, the internal regulator may become unstable.	Yes / No	
	Connection of reactance	Is reactance connected directly with power supply?	The characteristic of internal requlator might not be obtained by the reactance element.	Yes / No	If reactance is put directly in the power supply of chip , it is necessary to conect capacitor between chip power supply and reactance.
	Memory map	Are the operation checks made by enabling the guarded break for unused area conforming to the ROM and RAM amounts of the Flash and mask chips in the memory map for tool evaluation?	The built-in memory amount of the EVA chip for evaluation and that of the Flash and mask chip are different. Therefore, the actual chips may not work even if normal operation is confirmed by using a tool.	Yes / No	
	Stack usage	Is the maximum usage of stack confirmed?	Incorrect estimation of the stack usage could lead to RAM damage.	Yes / No	It is recommended to use the C analyzer of Softune to confirm the maximum usage of stack (Since the C analyzer cannot confirm a dynamic stack, it is necessary to consider the possibility of multiple interrupts when confirming the maximum usage).
	Read-modify-write related instructions	Is any instruction of the read-modify related operation executed for a register with write-only bits?	Since, when a read-modify-write related instruction (such as SETB) is used on a register with write-only bits, the read value of the write-only bit is undefined, problems may be caused (When safety use of the read-modify-write instructions is described in the manual for a register, no problem will be caused).	Yes / No	When developing with the C source, confirm whether any read-modify-write related instruction is executed for a register with write-only bits in units of bits in the header file as appropriate.
	Operation mode of tools	Is the operation confirmed by setting the operation mode to the native mode for final tool evaluation?	The native mode and debug mode are available as the operation modes of tools. Since the working speed in debug mode is different from the actual working speed, it is recommended to make an evaluation after setting the native mode.	Yes / No	
	HSTX pin	Are any measures taken for HSTX pin noise?	When any input less than 4tcp is made for HSTX pins, CPU standby mode cannot be released until the next regular HSTX input.	Yes / No	When an input less than 4tcp can be made for the HSTX pin, we recommend using a CPU operation monitor IC such as an external watchdog. (Using an internal watchdog built into the CPU alone will not release standby mode under these circumstances.)