

This check sheet is provided to prevent problems that may arise in the system development of MB90335series.
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Item	Content	Reason	Result	Remarks	
CPU	Power-on reset	Is the standard on electrical characteristics concerning power-on reset being met?	Powering on without meeting the power-on reset standard may result in the execution of commands by CPU without the power-on reset implemented normally.	Yes / No	Applied to systems using reset at power-on (Not applied to systems using power monitoring IC for reset equivalent input).
	External reset	Does the reset range meet the Fujitsu's standard?	When the reset range does not meet the Fujitsu's standard, recovery cannot be implemented.	Yes / No	
	Hard-wired reset	In FLASH micro computer, the values of reset vector and mode data are determined with an internal circuit. (Reset vector address: FFA000H, Mode data: 00H)	Unless the start address of a program is set to be the fixed vector address of hard-wired reset, the abnormal operation is implemented. Note that this failure is, however, not debugged with an Evaluation(EVA) chip.	Yes / No	
	Reset cause bits	When using the watchdog timer control (WDTC) register's reset cause bits, is the WDTC register read once by using the program default setting, followed by the clearing of the reset cause bits?	The default values of all reset cause bits are undefined. Accordingly, in order to clear all reset cause bits, ensure that the WDTC register is read once before using it.	Yes / No	Applied only when reset cause bits are used.
	PLL->Main	In software development, is attention given to the timing of the changes in the CPU's operation speed during the status transition of Main -> PLL -> Main -> PLL when such processing speed does change? (Is consideration given to the need to wait for eight cycles between MCS "1" write and "0" write?)	Within the eight cycles between MCS "1" write (Main) and "0" write (PLL), "0" write can be ignored.	Yes / No	Refer to the explanation of the MSC bit in the manual.
	PLL -> Stop -> PLL	For direct transition to PLL mode following the release of main clock stop status, is the oscillation stabilization wait time of the main clock set longer than the PLL clock wait time?	When transition to PLL mode recurs after transition from PLL mode to sub RUN (or STOP) status, the oscillation stabilization wait time of the main clock should be set longer than the PLL clock wait time.	Yes / No	
	Transition to standby mode	Do you know the notes to be followed at transition to standby mode?	For transition to standby mode, to access the low power consumption mode control register, add the following commands. <code>MOV LPMCR,#xch ;standby mode transition com.</code> <code>NOP</code> <code>NOP</code> <code>JMP S+3 ;jump to next com.</code> For details, see the hardware manual. (See the chapter on low power consumption mode.)	Yes / No	Applied only when standby mode is used.
Time-base timer	Do you know that the counter of the time-base timer is cleared automatically by hardware?	Since the time-base timer is used as a counter of the oscillation stabilization wait time and PLL clock stabilization wait time, the counter is automatically cleared in the following state transitions: - Transition from the main clock mode to the PLL clock mode - Transition to the stop mode Care needs to be taken when the time-base timer is used by software or the time-base timer is selected as the count clock of, for example, the PPG timer.	Yes / No		
I2C	Is INT bit cleared at the end of the interrupt routine processing?	SCL pin = LOW output in a state of "INT bit = 1" and making the SCL pin open when INT bit is cleared are specified. Therefore, it is necessary to perform I2C data processing in a state of "INT bit = 1" (SCL pin = LOW) and to clear INT bit (open SCL pin) when it becomes ready for sending or receiving the next piece of data.	Yes / No		

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	Is AL bit confirmed after setting the master mode (writing "1" to MSS bit)?	If the master mode is set ("1" is written to MSS bit) when the SCL pin or SDA pin is in "LOW" state, it becomes impossible to generate a start condition and output the SCL clock so that no transfer end interrupt (INT bit) occurs. Thus, after setting the master mode (writing "1" to MSS bit), wait for the 3 bit data transfer time and then check AL bit for this state (It takes the 3 bit transfer time after setting MSSbit = "1" for a change of AL bit).	Yes / No	Only when I2C is used
	Is any general call address sent in multimaster mode?	Since this product prohibits the kind of use in which general call addresses are sent and then lost in arbitration, it is recommended not to send any general call address in multi master mode.	Yes / No	Only when I2C is used
	Is the operating frequency of this product set so that the data setup time standard of its communication destination should be satisfied?	When this product is used at 20 MHz or below, the minimum data setup time is 250 ns. When the frequency used exceeds 20 MHz, the minimum data setup time is 200 ns. Thus, set the operating frequency of this product by adjusting to the data setup time standard of its communication destination.	Yes / No	Only when I2C is used
	When using the I2C bus, are the dual-purpose pins P66, P67, PB0, PB1, PB2, and PB3 used by setting them for input (DDR=0)?	When RMW instruction is executed on the same series (P60 to P67 or PB0 to PB6) as the dual-pin (P66/SCL0, P67/SDA0, PB0/SCL1, PB1/SDA1, PB2/SCL2, PB3/SDA2) with the I2C bus and the dual-purpose pin is set for output, PDR66, 67, B0, B1, B2, or B3 may change due to execution of the RMW instruction. When the I2C bus is prohibited in this state, the changed value of PDR66, PDR67, B0, B1, B2, or B3 is output to a port.	Yes / No	Only when I2C is used
USB	Are not you expecting VON, VOFF setting to be able to be detected with the VBUS(UTEST) pin even in the state of the USB suspend?	There is no adverse effect in the USB communication though VOFF and VON cannot be detected with the VBUS pin in the state of the USB suspend. However, please use the external interruption pin instead whenever it is necessary to always observe VBUS as LED is turned off when disconnecting it with the host on customer's system.	Yes / No	Only when VBUS(UTEST) pin is used
	Do you connect the pull-down resistance with the VBUS(UTEST) pin?	Please connect the pull-down resistance because this pin is an input pin.	Yes / No	
	When USB Mini-HOST is used, are you setting the EOF setting register referring to the example of calculating microcontroller's hardware manual	There is a possibility that SOF is missed because Mini-Host does not have the margin when setting it according to the calculation type of USB specifications.	Yes / No	Only when USB Mini-HOST is used
	Are not you changing the microcontroller to the standby mode while transferring USB?	The microcontroller is prohibited from changing it to the standby mode while transferring USB.	Yes / No	Only when USB is used
	When using USB, is the clock set to 6 MHz multiplied by four?	To use USB, the clock should always be set to 6 MHz multiplied by four.	Yes / No	Only when USB is used
Unused pin treatment	Is any unused pin pulled up or pulled down by the resistor of 2 k or more? Or, is the port output treatment performed in the initial routine by leaving the pin opened?	When an unused pin is treated without a resistor and the port level opposite to the processing level is output due to CPU runaway, problems such as latch-up may arise.	Yes / No	
Interrupt	Is the interrupt vector processing of an exceptional interrupt performed?	Runaway may be caused when an undefined instruction is executed due, for example, to runaway.	Yes / No	When an undefined instruction is executed, an exceptional interrupt occurs. Thus, when special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended.
	Are interrupt factors cleared in the main routine?	Since interrupt factors may be cleared and set simultaneously, it is recommended to clear interrupt factors in an interrupt routine. When interrupt sources are to be cleared in the main routine, it is recommended to clear them after prohibiting interrupts of the target peripheral.	Yes / No	Since, particularly for UART, reception interrupts are set asynchronously, it is recommended to clear interrupt factors in an interrupt routine so that they should not occur simultaneously with reception interrupt setting or clear them after prohibiting reception interrupts.
	Is processing of an unused interrupt vector performed?	Runaway may be caused when an unused interrupt occurs due, for example, to runaway.	Yes / No	When special processing is needed, jump to the processing. When no special processing is needed, jumping to a reset vector is recommended

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	Bit manipulation instruction	Read-modify instruction is prohibited by some registers of each resource. Is any RMW instruction used in the target register?	The instruction may not be executed normally, resulting in unintended data being written.	Yes / No	Read-modify-write related instruction is indicated in the instruction list by * in RMW.
	Main clock oscillation stabilization wait	Is the required oscillation stabilization wait time identified by obtaining matching data of the system and oscillator?	CPU may be run before oscillation has stabilized.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.
	Watchdog	Is the watchdog timer cleared by, for example, a timer interrupt? (Are incorrect PLL multiplication settings and the intermittent operation mode considered?)	When the watchdog reset interval is not sufficient, whether a program is proceeding normally cannot be detected.	Yes / No	
	External reset IC	When using external reset IC, is the low-voltage detecting value within the guaranteed operation voltages of the microcomputer? Is the voltage drop between detection and reset considered?	When no reset within the guaranteed operation voltages is entered, a malfunction may occur.	Yes / No	Confirm the guaranteed operation voltage range in the data sheet.
	I/O port	Is processing such as additional writing performed for the purpose of a fail-safe system in important port input/output?	Basically, the port state does not change as long as not set by software. However, for the purpose of making the system fail-safe, it is recommended to insert software of a refresh function such as additional writing into important ports.	Yes / No	
		When using the CMOS I/O port for output, is the DDRx register set after setting the PDRx register?	Since the initial value of the PDRx register is undefined, if the DDRx register is set for output without setting the PDRx register, the output becomes undefined. Before setting the DDRx register for output, set the PDRx register first.	Yes / No	
	Flash	When users are allowed to write to FLASH memory in user programming mode, is the hardware sequence flag used to control writing to FLASH memory?	Since the FMCS register cannot be used to check for write/delete errors, it is recommended to use the hardware sequence flag to control writing to/deleting FLASH memory.	Yes / No	Only when FLASH memory is written to by the user
General	Do the voltage, ambient temperature, and operating frequency ranges satisfy the standards specified by Fujitsu? When any of them does not satisfy the standards, is any special guarantee considered and supported?	When not used within the guarantee range, no product guarantee can be provided.	Yes / No	Check the guaranteed operation range in the data sheet.	
	When a special guarantee is considered, is a notification form returned to the Sales Dept. after affixing a "confirmation stamp (No problem, Problem found) in the reply" on the notification form?	If a special guarantee is provided, test changes may be needed. Thus, make sure to return the notification form before ROM release.	Yes / No	Since it may take up to several months to deal with test changes, they may not be dealt with when the notification form is returned just before ROM release.	
Noise reduction measures and others	Mode(MOD) pin	Is the same level for processing of the MOD pin ensured even while executing instructions?	The level of the MOD pin may be read incorrectly (When a high-impedance resistor is used for treating the MOD pin, the MOD pin level may not be ensured due to noise).	Yes / No	When external noise tends to propagate to the MOD pin, it is recommended to take countermeasures against static electricity such as connecting a capacitor to the mode pin.
		Is interconnect for treating the MOD pin too long or is there any adjacent high current signal interconnect?	The level of the MOD pin may be read incorrectly due to power supply deviation and noise.	Yes / No	
	Oscillation	When using a crystal oscillator, is an appropriate dumping resistor inserted?	To use a crystal oscillator, a dumping resistor to reduce the excitation current is needed.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.
		Is oscillation matching data of mass-produced products obtained?	Since oscillation characteristics of flash products and those of mask products may be different, it is recommended to obtain oscillation matching data of mass-produced products.	Yes / No	Make a request of the oscillation evaluation to the manufacturer of the oscillator to be used.
		Is the resistance of the dumping resistor for the oscillation circuit determined in view of unnecessary radiation noise and oscillation amplitude?	When oscillation is abnormal or an overshoot or undershoot of oscillation occurs, unnecessary radiation noise may increase.	Yes / No	When a problem of unnecessary radiation noise arises, it is necessary to first confirm the oscillation waveforms and then examine whether to insert a dumping resistor as a measure to reduce unnecessary radiation noise.
		Is the oscillator arranged as close to the chip as possible?	CPU runaway due to external noise may be presumed.	Yes / No	It is recommended to arrange the oscillator as close to the chip as possible?
	Vcc, GND	Is consideration given to making Vcc and GND as strong as possible?	Problems of unnecessary radiation noise and CPU runaway due to external noise may be presumed.	Yes / No	To avoid problems of unnecessary radiation noise and external noise, it is recommended to take the power supply and GND as widely as possible (By arranging GND under the chip, for example, the GND can be strengthened).

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ESD, latch-up, noise	Are mass-produced chips used to evaluate ESD, latch-up, and noise resistances?	Since the resistances against ESD, latch-up, and noise of Flash products and those of mask products are different, it is recommended to use mass-produced products to evaluate ESD and latch-up resistance.	Yes / No	Since it is possible to submit measurement results of Fujitsu as characteristic examples of resistance characteristic data between MASK and FLASH products, make a request of them.
Capacitor	Is the optimum capacitor connected near the chips as a capacitor for reducing noise?	The capacitor connected to reduce noise may not work with reactance components of interconnect(Measures that take noise components into account are needed).	Yes / No	
Connection of reactance	Is reactance connected directly with power supply?	The characteristic of internal regulator might not be obtained by the reactance element.	Yes / No	If reactance is put directly in the power supply of chip, it is necessary to connect capacitor between chip power supply and reactance.
Memory map	Are the operation checks made by enabling the guarded break for unused area conforming to the ROM and RAM amounts of the Flash and mask chips in the memory map for tool evaluation?	The built-in memory amount of the EVA chip for evaluation and that of the Flash and mask chip are different. Therefore, the actual chips may not work even if normal operation is confirmed by using a tool.	Yes / No	
Stack usage	Is the maximum usage of stack confirmed?	Incorrect estimation of the stack usage could lead to RAM damage.	Yes / No	It is recommended to use the C analyzer of Softune to confirm the maximum usage of stack(Since the C analyzer cannot confirm a dynamic stack, it is necessary to consider the possibility of multiple interrupts when confirming the maximum usage).
Read-modify-write related instructions	Is any instruction of the read-modify related operation executed for a register with write-only bits?	Since, when a read-modify-write related instruction (such as SETB) is used on a register with write-only bits, the read value of the write-only bit is undefined, problems may be caused (When safety use of the read-modify-write instructions is described in the manual for a register no problem will be caused).	Yes / No	When developing with the C source, confirm whether any read-modify-write related instruction is executed for a register with write-only bits in units of bits in the header file as appropriate.
Operation mode of tools	Is the operation confirmed by setting the operation mode to the native mode for final tool evaluation?	The native mode and debug mode are available as the operation modes of tools. Since the working speed in debug mode is different from the actual working speed, it is recommended to make an evaluation after setting the native mode.	Yes / No	