EDID Memory LSI with 4 DDC (I^2C) Ports for Digital TVs MB85RF402

This product is an EDID memory for display supporting HDMI such as digital TVs, etc., and is applying FRAM in the nonvolatile memory area.

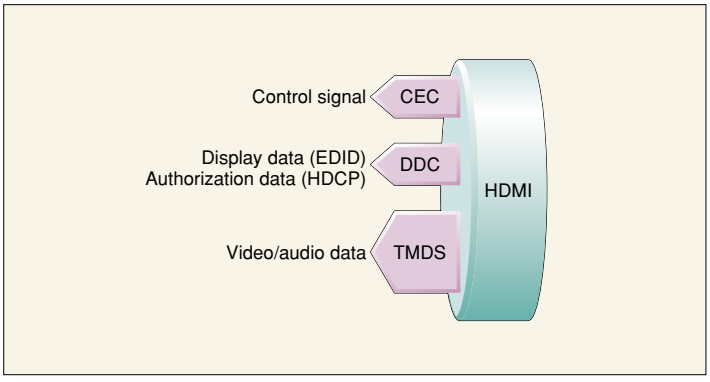
* FRAM: Ferroelectric Random Access Memory
* EDID: Extended Display Identification Data

Overview

This product is an EDID memory for digital TVs that adopts 256-word×8-bit FRAM and 4 built-in DDC (I^2C) ports as the output interface.

The currently available digital TVs are equipped with HDMI (High-Definition Multimedia Interface) terminals. HDMI is capable of contents protection and the simultaneous transmission of uncompressed images and multi-channel audio. Devices that utilize HDMI for output include DVD players, DVD/HDD recorders, next-generation DVD devices incorporating Blu-ray or HD-DVD as well as recent digital video cameras and video game consoles. As the outputting devices expand, the number of HDMI ports equipped on digital TVs has also been increasing.

Figure 1 HDMI Schematic Drawing

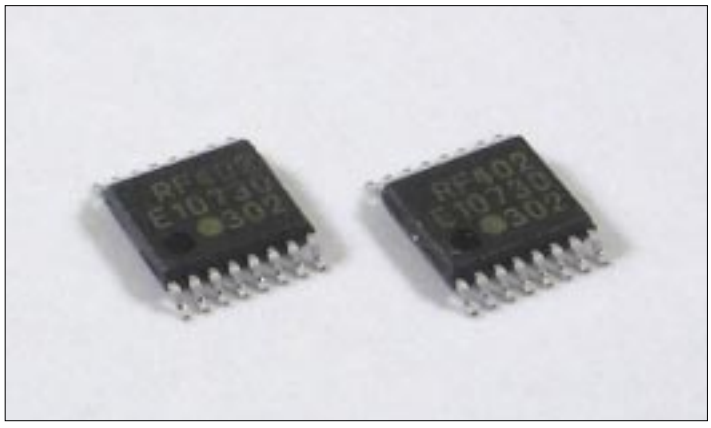


HDMI has 3 built-in transmission paths: TMDS, DDC, and CEC.

Fig.1 presents the schematic diagram of HDMI. TMDS transmits image and audio data, and DDC is used for the transmission of EDID (the display data) as well as HDCP (High-bandwidth Digital Content Protection) authentication that protects the contents. CEC (Consumer Electronics Control) is used to transmit device control signals such as remote controller signals so that all devices can be controlled with a single remote controller when the supporting devices are connected.

Display data EDID indicates the resolution and supported functions. Thus, the display device such as a digital TV must

Photo 1 External View



be able to read EDID from each HDMI port. Although it has been conventional to mount 1 E^2PROM for each HDMI port, it is now possible to provide EDID on one chip for up to 4 HDMI ports by adopting this product.

Features

Main specifications

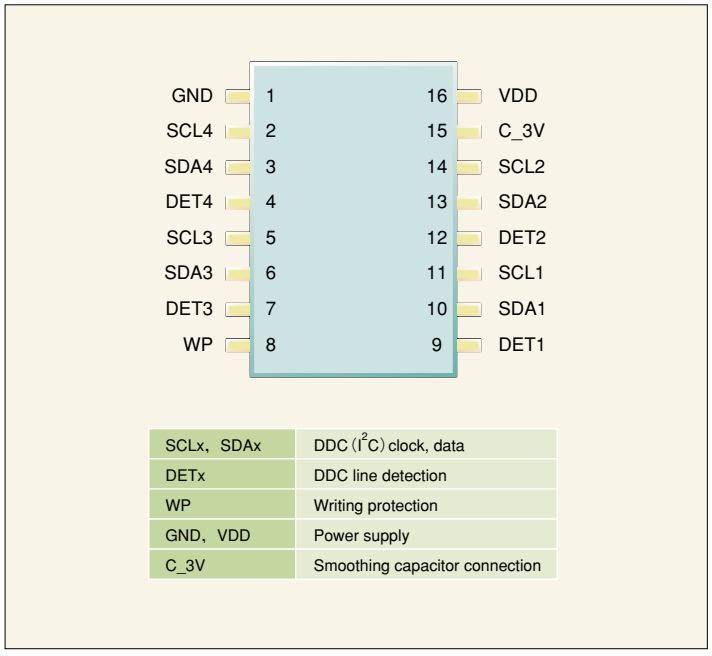
- Memory size: 256-word×8-bit
- Power supply voltage for operation: 3.8V to 5.5V
- Read/write endurance: 10^{10} times
- Package: TSSOP 16
- Current consumption: 600μA during operation (typical value)
- At standby: 25μA (typical value)

Fig.2 presents the pin assignments.

Built-in 4-port DDC (I^2C) interface

This product has a built-in 4-port DDC (I^2C) interface and reading/writing is possible from any of the ports. In addition, all of the ports support I^2C Standard-mode (100kbps) and Fast-mode (400kbps) and an arbitration circuit is equipped internally to enable simultaneous access. Arbitration operation is not externally visible due to the high-speed accessing of FRAM when the ports are accessed by DDC (=I^2C Standard-mode), which is normally used in HDMI.

Figure 2 Pin Assignments



SCLx, SDAx	DDC (I^2C) clock, data
DETx	DDC line detection
WP	Writing protection
GND, VDD	Power supply
C_3V	Smoothing capacitor connection

Low power consumption

The current consumption during operation is 600μA (typical value) for both reading and writing, and the current consumption for writing is dramatically lower than that of E^2PROM (several milliamps). Although it is equivalent to E^2PROM in reading, it is relatively small due to the high-speed accessing of FRAM.

Automatic detection and output conversion functions of HDMI VSDB (Vendor-Specific Data Block)

The superlative feature of this product is the automatic HDMI VSDB detection and output conversion functions. One of the data types to be written in EDID is HDMI VSDB specified by HDMI standard. HDMI VSDB has a field called Source Physical Address (hereafter referred to as "Physical Address") where the data indicating the address of the device connected to the HDMI port is written. This address is used to control other devices with HDMI connection using CEC. When several HDMI ports are to be equipped on a digital TV, a different address must be assigned to each of the HDMI ports. Conventionally, E^2PROM was used for each HDMI port and each E^2PROM had different data only in 2bytes for the Physical Address and the checksum for the corresponding area.

This product is equipped with a function to automatically detect the Physical Address and output the data corresponding to the accessed port when there is an access to a Physical Address. This function enables the function conventionally realized by 4 E^2PROMs to be achieved on one chip. Similarly, it outputs the data for the checksum for the area corresponding to the Physical Address that corresponds to the accessed port.

Functions

This product accesses FRAM from the DDC (I^2C) port.

Fig.3 presents the block diagram. This product has only one 2K-bit FRAM as the memory size for the 4 DDC (I^2C) ports. While up to 2K-bit×4 (total of 8K-bit) memory size was necessary in conventional products, the same function can be realized with only one chip of this product (2K-bit).

Furthermore, FRAM access is arbitrated by the access control block to enable simultaneous access to the 4 ports. However, under conditions of normal use, from the outside it appears as if it is operating simultaneously due to the high-speed accessing (570ns in 1 access <typical value>) of FRAM compared to the DDC speed of 100kbps. In addition, the DDC port is I^2C - compatible. It supports Standard-mode (max. 100kbps) as well as Fast-mode (max. 400kbps) when used as I^2C.

Application Examples

Fig.4 ports in a digital TV with multiple HDMI ports. It is also possible to connect one of the ports to the internal microcontroller exclusively for writing. Furthermore, the same port can be used as the writing port and DDC port for EDID output for HDMI by providing a switching mechanism.

Future Development

Over 500 million units of our FRAM products have been shipped so far. We developed this product as FRAM ASSP with HDMI to be equipped on digital TVs. In the future, we will devote our efforts to expanding the lineup so that FRAM can be used in various applications. ✱

NOTES

* DDC and EDID are trademarks of Video Electronics Standard Association (VESA).
* HDMI, the HDMI logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC.

Figure 3 Block Diagram

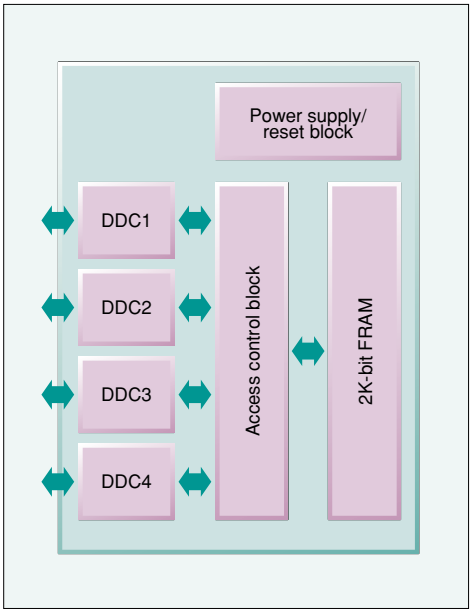


Figure 4 Configuration Image