Innovative Fast Timing Design Solution through Simultaneous Processing of Logic Synthesis and Placement

New AccelArray™ Design Flow

A new design methodology is now available that offers the advantages of enhanced logical design efficiency at customer sites and reduced time to market for cutting-edge technology structured ASICs which implement the required functions faster at lower cost.

Overview

AccelArray, FUJITSU’s innovative structured ASIC dramatically reduces product development costs and time to market while providing high performance because its platforms come with a common base master and simplified design tasks. In addition to these features, FUJITSU now delivers a design flow to streamline logical design, timing design in particular, at customer sites.

This new design flow provides the benefits listed below for

Figure 1 Design Flow and Handoff

Master data

Increased estimation reliability through careful layout consideration

Reduced uncertainty and consequently increased TAT accuracy

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Possible rework required due to insufficient layout consideration
product development at customer sites.

- **Logical design is carried out while taking into account the LSI timing operation even at the earliest stage of development**
- **Reduced period of time from handoff to sample delivery and a consequently enhanced scheduling reliability**

In order to implement the new design flow, FUJITSU has developed Amplify® AccelArray Pro, a physical synthesis tool optimized for AccelArray, in cooperation with Synplicity, Inc., an EDA (Electronic Design Automation) tool vendor in the US that offers logical synthesis tools for FPGAs and ASICs. This tool is available bundled with the AccelArray design kit to help our customers to save tool costs.

**Development Based on Logic Synthesis by “Conventional Design Flow”**

In the typical flow of ASIC development, FUJITSU is responsible for all layout processing (placement and routing) for the cell-based Netlist supplied by the customer. In this design flow, the timing design in the stage of logical design at the customer site is based on the statistical wire capacitance table. The statistical wire capacitance table is designed on the basis of statistical data for ASIC development at FUJITSU to ensure higher correlation between the timing estimation in the logical design at the customer site and the actual timing after layout.

In practice, however, this table refers to statistical data and thus it is not always suited to the LSI actually developed by the customer. The layout task for the Netlist submitted by the customer sometimes takes a lot of time in order to satisfy the timing constraints—this can pose a threat to the customer’s product development schedule (left-hand diagram in Fig. 1 and left-hand diagram in Fig. 2).

In addition, in order to reduce the aforementioned schedule disruption risk, development is typically carried out with feedback regarding the result of layout prototyping to logical design from the earliest stage of development between the customer and FUJITSU; this can affect the design efficiency and controllability of the design process (Fig. 3).

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**Figure 2** Timing Estimation

**Figure 3** Typical Development Process
Development Based on the Simultaneous Processing of Logic Synthesis and Placement Using the New Design Flow

The new design flow of AccelArray helps minimize the above-described risk and streamline the timing design in particular.

In the new design flow, the creation of the RTL (Register Transfer Level) by the customer is followed by physical synthesis (logic synthesis+placement). Physical synthesis creates a cell-based Netlist in a similar manner as logic synthesis. In addition, in conjunction with logic synthesis, cell placement is determined on the master (frame) selected by the customer.

In the stage of physical synthesis and also in the timing analysis, on the basis of the placement determined by physical synthesis and the estimated wiring route in consideration of the available wiring resources on the master, the wiring capacitance and resistor value are calculated in order to implement the analysis for the layout as close as possible to the actual conditions (right-hand diagram in Fig.1 and right-hand diagram in Fig.2).

Also in the layout task at FUJITSU after handoff, reduced layout task time and increased task schedule accuracy up until sample shipment are achieved since the timing convergence and the possibility of wiring accommodation have already been verified during physical synthesis at the customer site.

As such, the design flow using physical synthesis provides the following benefits:
Increased timing design and estimation reliability at the customer site

- Earlier identification of any timing design for which emphasis is to be placed for proper adjustment
- Elimination of any timing design that may be left out of the adjustment

Allowable checking for the possibility of wiring accommodation at the customer site

- Early identification of tradeoffs between the amount of logics incorporated, timing, and the possibility of wiring accommodation
- Reduced iteration of feedback from FUJITSU

Reduced time to sample shipment from the handoff to FUJITSU and increased time schedule accuracy

- Reduced time to market at the customer site
- Increased time for focusing on product function development at the customer site

As a result, in the design process throughout the product development at the customer site, feedback iteration from layout prototyping between the customer and FUJITSU is reduced and design process controllability is enhanced (Fig.4).

**AccelArray™ Design Kit**

As a design kit for the new design flow based on physical synthesis, FUJITSU offers the following tools (only pertinent to physical synthesis):

- **RTL checker (under development):** Checks AccelArray-specific design rules on the RTL
- **DDR I/F compiler:** Creates the I/F module that has guaranteed timing operation
- **RAM compiler:** Creates the RAM module that allows mapping to the master (frame)
- **Pin assignment support tool:** Supports and checks pin assignment
- **Master data creation tool:** Creates the master data for physical synthesis
- **Amplify AccelArray Pro:** Physical synthesis specifically intended for AccelArray

Fig.5 presents the flow of RTL design tasks, and Fig.6 presents the flow of physical synthesis tasks.

The DDR I/F compiler creates the DDR I/F module macros that guarantee the timing operation after layout by entering the customer’s DDR I/F specifications. In addition, a RAM compiler to expand the bit/word configuration RAM module

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**Figure 6 Flow of Physical Synthesis Tasks**

- **RTL design task**
- **Pin & I/O assignment task**
- **RTL description**
- **RTL description check**
- **Physical synthesis (Logic synthesis + Placement)**
- **Handoff check**
- **Netlist**
- **Assignment**
- **Pin assignment support tools**
  - Available pin assignment template
  - Visualized I/O placement and bump location
- **RTL checker (under development)**
  - AccelArray-specific design rules to be checked on the RTL
- **Master data creation tools**
  - Placement of I/O, PLL, and other IP macros
  - Creation of master (frame) data for physical synthesis
- **Amplify AccelArray Pro**
  - Automatic RAM placement
  - Logic synthesis + Placement + Timing optimization
- **Handoff checker**
  - Netlist checking
  - Placement checking (under development)
macros using the RAM element incorporated in AccelArray is commercialized. Conventionally, ASICs require DFT (Design for Test) synthesis to insert the DFT circuits into the Netlist supplied by the customer, whereas AccelArray involves only limited insertion of DFT circuits and simplified checking for DFT conformity, which contributes to the reduction in logical design time.

Fig.7 presents the features of Amplify AccelArray Pro. Amplify AccelArray Pro is a physical synthesis tool optimized for AccelArray. It has been developed under close cooperation between FUJITSU and Synplicity, Inc., an American EDA tool vendor that supplies logical synthesis tools for FPGAs and ASICs. The placement engine and the timing optimization engine are optimized for the AccelArray chip architecture. The timing estimated by the Amplify AccelArray Pro demonstrates higher correlation with the final wire-routed layout, and successfully realizes single-path design from logical design through layout.

Fig.8 presents a typical Amplify AccelArray Pro evaluation result. The vertical line refers to the timing slack value for the path estimated by the Amplify AccelArray Pro during physical synthesis, and the horizontal line refers to the value after layout. Each dot represents a slack value of one path, and a closer correlation holds as the plot approaches the straight line extending from the bottom left to the top right. When the plot lies below the correlation line, it indicates that the slack values estimated by the Amplify AccelArray Pro are not excessively optimistic against those after layout. This suggests that the timing critical region shows higher correlation and that the estimation does not provide any optimistic results.

The Amplify AccelArray Pro allows batch synthesis of circuits for gate size exceeding 4M, thus assuring efficient timing design of the entire design.

Layout Task after Handoff

Fig.9 presents the layout task at FUJITSU after handoff. In conventional ASIC design, insertion of the DFT circuit, design of power supply and the creation of clock trees follow the supply of design data from the customer. In the AccelArray, these circuits are already embedded in the master in the optimized state and thus, in the layout design, the customer circuit is mapped onto the embedded circuits, through which low clock skew, DFT timing design, and signal-integrity-verified layout design can be realized.

In the new design flow, for customer circuit and RAM placement data as well, the layout time may be further reduced by mapping the results of physical synthesis at the customer site to the master.

Specifications

AccelArray adopts cutting-edge technology, the incorporation of a fast interface IP (3.125Gbps), and mounting in an FC-BGA package of ultrahigh density in order to accommodate high speed and multiple signals, providing high performance. It may also be applicable to those domains in which the performance and cost requirements cannot be satisfied by FPGA.

- **Product name:** AccelArray
- **Type:** MBCA91xxx-yyy (xxx refers to the name of the frame, yyy refers to the product identification number, both of which are specified by FUJITSU.)
- **Process technology:** 0.11μm Si gate-CMOS, 6 to 7 interconnect
layer wiring (copper wire), Low-k Interlayer Dielectric structure, area bump

- Max. operating frequency: 333MHz
- Supply voltage (Basic specifications): 1.2V±0.1V/2.5V±0.2V (Dual power supply)
- Basic interface: 2.5V CMOS, 3.3V Tolerant

**Configurable IP macros and I/Os**
This product supports the following IP macros and I/Os: RAM (1R1W, 2RW), DDR I/F, PLL (output frequency 25 to 800MHz), ARM9, 2.5V-LVCMOS/3.3V-Tolerant, HSTL, PCML, LVDS, SSTL2, PCI-66, PCI-X, SPI-4P2, XAU1, BackPlane, SGMII/1GBASE-LX/SX, and PCI-Express
Functional IPs applicable with a standard cell are all supported (including those under development).

**Package**
To accommodate ultrahigh-speed, multiple-signal, and large current consumption applications, area bump is adopted in the chip, and the package is of ultrahigh-density FC-BGA type.

**Frame lineups**
- Mega frame: Standard product
  : Configured with ARM9
- Giga frame: Configured with a high-speed interface

*Table 1 presents a lineup of mega frames, and Table 2 provides a lineup of giga frames.*

**Summary**
FUJITSU has introduced new design flow that further streamlines logical design, timing design in particular, and faster development turnaround, by physical synthesis tools in the AccelArray, the high-performance structured ASIC, which simultaneously performs logic synthesis and placement to provide our customers with design flow. FUJITSU will continue to develop design flow and LSI products that appeal to the product development of individual customers.

**NOTES**
* AccelArray is a trademark of FUJITSU LIMITED.
* Amplify is a registered trademark of Synplicity, Inc.
* All company and product names contained herein may be trademarks or registered trademarks of their respective companies.
## Table 1 Mega frame Lineup

<table>
<thead>
<tr>
<th>Frame Name</th>
<th>M20</th>
<th>M30</th>
<th>M40</th>
<th>M50</th>
<th>M52</th>
<th>A50</th>
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<tbody>
<tr>
<td>I/O cell count</td>
<td>696</td>
<td>824</td>
<td>952</td>
<td>1176</td>
<td>1176</td>
<td>1176</td>
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<tr>
<td>FF cell count (×1,000)</td>
<td>50</td>
<td>70</td>
<td>93</td>
<td>150</td>
<td>233</td>
<td>186</td>
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<tr>
<td>Raw gates (×1,000)</td>
<td>720</td>
<td>1008</td>
<td>1344</td>
<td>2160</td>
<td>3689</td>
<td>2872</td>
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<tr>
<td>Number of gates in terms of ASIC (×1,000)</td>
<td>1219</td>
<td>1707</td>
<td>2276</td>
<td>3658</td>
<td>6019</td>
<td>4736</td>
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<tr>
<td>SRAM size (Kbit)</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2RW-SRAM</td>
<td>1680</td>
<td>2240</td>
<td>2880</td>
<td>4400</td>
<td>2400</td>
<td>2960</td>
</tr>
<tr>
<td>1R1W-SRAM</td>
<td>90</td>
<td>105</td>
<td>120</td>
<td>150</td>
<td>150</td>
<td>150</td>
</tr>
<tr>
<td>Total (Max.)</td>
<td>1770</td>
<td>2345</td>
<td>3000</td>
<td>4550</td>
<td>2550</td>
<td>3110</td>
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<tr>
<td>Number of PLL macros</td>
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<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Package</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Body size shown in parentheses</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ball pitch 1.00mm</td>
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</tr>
</tbody>
</table>

* A50 frame is configured with ARM9 core.
* Available I/O count depends on the type of interface incorporated.

## Table 2 Giga frame Lineup

<table>
<thead>
<tr>
<th>Frame Name</th>
<th>G30</th>
<th>G40</th>
<th>G45</th>
<th>G50</th>
<th>G55</th>
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</thead>
<tbody>
<tr>
<td>4-channels G-phy (Tx + Rx)</td>
<td>3</td>
<td>4</td>
<td>2</td>
<td>6</td>
<td>2</td>
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<tr>
<td>S-phy (Tx + Rx)</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>I/O cell count (High-speed IF not included)</td>
<td>612</td>
<td>688</td>
<td>554</td>
<td>864</td>
<td>760</td>
</tr>
<tr>
<td>FF cell count (×1,000)</td>
<td>69</td>
<td>93</td>
<td>93</td>
<td>206</td>
<td>149</td>
</tr>
<tr>
<td>Raw gates (×1,000)</td>
<td>1007</td>
<td>1343</td>
<td>1343</td>
<td>3133</td>
<td>2158</td>
</tr>
<tr>
<td>Number of gates in terms of ASIC (×1,000)</td>
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<td>2275</td>
<td>2275</td>
<td>5196</td>
<td>3656</td>
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<tr>
<td>SRAM size (Kbit)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2RW-SRAM</td>
<td>1960</td>
<td>2560</td>
<td>2560</td>
<td>3040</td>
<td>4000</td>
</tr>
<tr>
<td>1R1W-SRAM</td>
<td>45</td>
<td>52</td>
<td>52</td>
<td>75</td>
<td>67</td>
</tr>
<tr>
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<td>2612</td>
<td>2612</td>
<td>3115</td>
<td>4067</td>
</tr>
<tr>
<td>Number of PLL macros</td>
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<td>8</td>
<td>8</td>
<td>8</td>
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</tr>
<tr>
<td>Package</td>
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