The SoC is an advanced set-top-box decoder designed to meet the needs of tomorrow's set-top-box market. The SoC includes advanced features to support multi-standard decoding of H.264, MPEG2, MPEG-4 and AVS, it supports hardware DMA, and encryption. A 324MHz ARC4 Tangent CPU with a 8Kbyte data and 8Kbyte instruction cache is included. The CPU is connected to a shared DDR2-SDRAM. Supporting the system is an advanced hardware acceleration unit capable of performing DMA operations including complex operations such as Triple DES encryption/decryption and RGB to 4:2:2 color space conversion. The system is optimized for PVR applications with two MPEG2 video decoders and output units, two independent transport stream decoders and a hardware DMA controller. The SoC comes with the Fujitsu Driver Application Programming Interface (FAPI) to help customers achieve the shortest possible development cycle. FAPI is a complete driver set allowing fast and efficient customer software design.

**Features**

- **System**
  - ARC TangentA4 CPU @ 324MHz
  - Bootable from from multi-bit Serial Flash
  - DDR2-667 SDRAM memory interface
- **Video/Audio**
  - QAM demodulator with DVB-C (ETS300-429) and ITU-T J83 annex A/C compatible, 10-bit ADC input
  - Two transport stream decoders, 2 DVB descrambler
  - 2nd hardware MPEG2 video decoding
  - 2 flexible MPEG video resizing units (factor 1/16 to 2)
  - 3-layer display controller (true-colour or CLUT)
  - High-performance 2D graphics accelerator
  - 2D de-interlacer for video interlaced to progressive conversion
  - Flexible frame rate conversion (50/60Hz), Flicker and Flutter fixer for better on-screen clarity
  - PAL/NTSC/SECAM digital encoder, incl Teletext / WSS / VPS / CC / VBID insertion, RGB De-matrix (RGB or YCrCb output)
  - Audio decoder: Programmable audio decoder supporting MPEG1 layer 1, 2 and 3 (MP3), HE-AAC, and others
- **Interfaces**
  - HDMI link and PHY
  - ITU-R 656 video input/output
  - video DACs for YPrPb/RGB, YC and CVBS
  - S/P-DIF output for PCM/AC3/MPEG, Dolby Digital 5.1
  - USB 2.0 incl. PHY (host or device)
  - Ethernet 10/100 Base-T MAC (RMII)
  - Shared GPIO, UART, 2xSmart Card, I2C, PWM, 7 segment LED, 5 digit keypad controller, IR, SDIO
  - On-chip PLL (48.0MHz crystal required)
- **Package/Technology**
  - QFP256 Package
  - Fujitsu 90nm technology

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**Diagram**

The diagram illustrates the internal architecture of the MB86H06 Multi-Standard Decoder for Set-Top-Boxes, including components such as ARC CPU, Audio Decoder Processor, Video Decoder Processor, Baseband Video Processor, DDR2 Memory Controller, QAM Demodulator, Transport Stream, Ethernet MAC, USB2.0, eFuse, Peripheral Interface, Universal Processor Interface, HDMI Link, Video DACs, HDMI Link + PHY, 2D Graphics Engine, DDR2 RAM, IF in, MI, S/P DIF, FS, LR, 1656 in, 1656 out, SD, HD, HDMI.
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