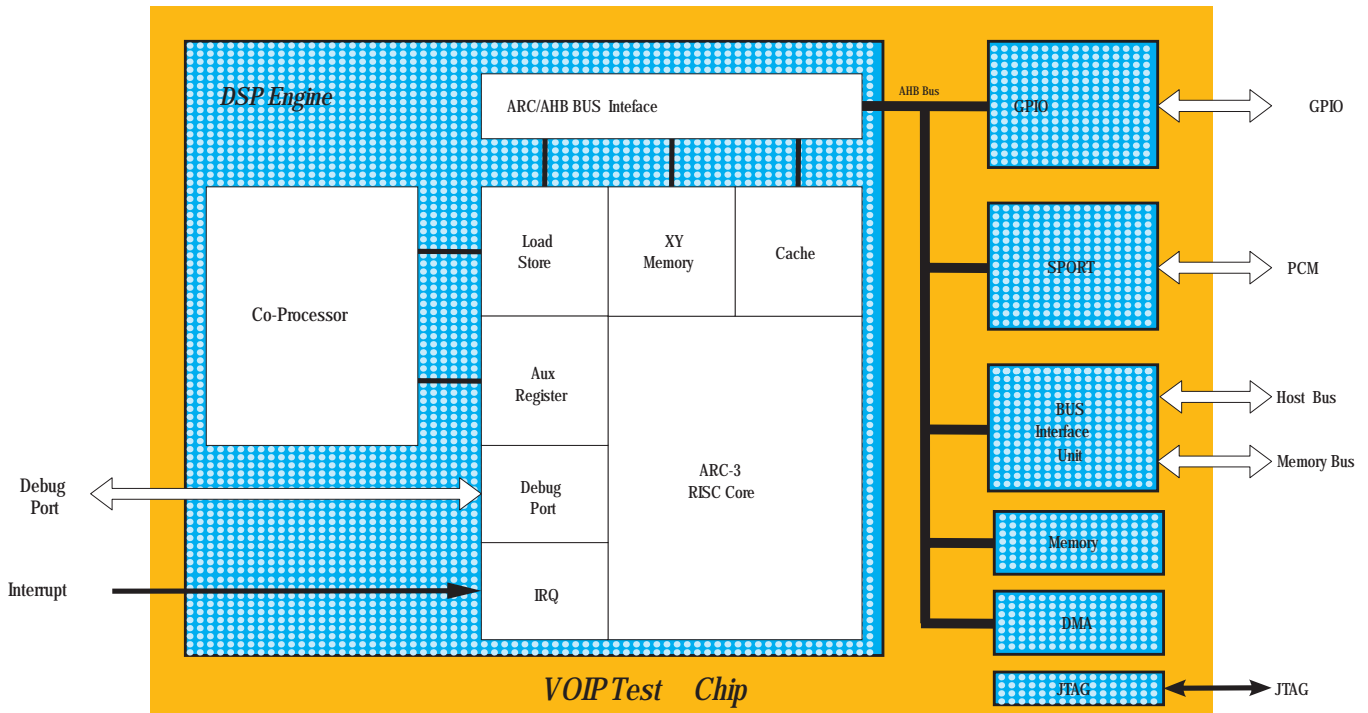


# Media Access IP: VoIP



## Features

- Four simultaneous and independent voice channels each supports
  - G.168 Echo Cancellation
  - Vocoders: G.711, G.726, G.728, G.729AB, G.729e
  - DTMF encode and DTMF decode
  - Dial tone generation
  - Reverse ring-back generation
- Bus master interface with built in DMA for accessing host and system memory. Shared system memory eliminates need for dedicated memory
- PCM Audio CODEC interface (SPORT) with AC'97 compliant audio CODEC
- Extended ARC-3 DSP core with Co-Processor provides efficient & flexible soft solution for algorithm updates and optimization
- Complete evaluation system
- Boundary scan test (JTAG)
- 3.3V I/O, 2.5 V Core, 0.25 $\mu$ m technology (Test chip)
- 304 PQFP (Test chip)

## Overview

VoIP Codec is designed for implementing speech Vocoders to support VoIP applications for Customer Premises Equipment (CPE). Up to 4 channels of audio can be supported simultaneously.

The current implemented Vocoders are G.711, G.726, G.728, G.729AB, and G.729E. Any combination of Vocoders is supported and each channel provides echo cancellation (G.168), DTMF generation/detection, and jitter buffering.

The DSP Engine is based on ARC-3 Processor utilizing its DSP (Co-Processor). A complete system designed around Raptor Test Chip is also available for evaluation purposes only to provide a home gateway solution. This system uses an ARC-3 processor as its host to run application software with a real time operating system, network stack and MGCP protocols.

## ARC DSP Engine

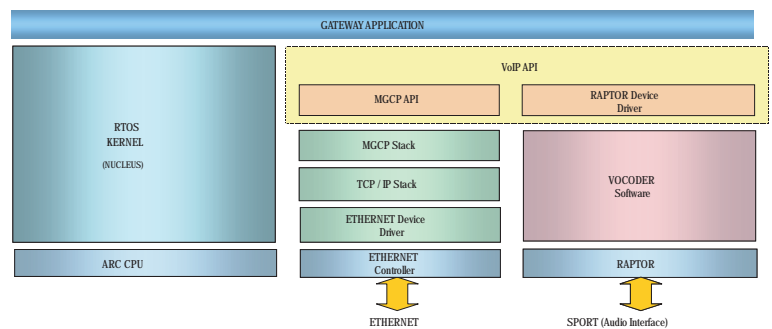
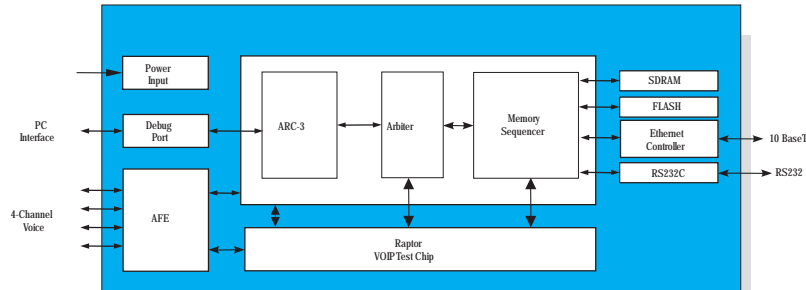
DSP engine provides the means for in-line and parallel acceleration of algorithms. In-line acceleration is accomplished through the addition of select instructions to the ARC execution unit while parallel acceleration is accomplished through a Co-Processor unit. DSP engine consists of a baseline ARC 3.0 core with several additional features and extensions.

### DSP Configuration:

- Dual 16x16 XMAC
- Saturated add/subtract
- X-Y memory and associated controller supports 16 and 32-bit data addressing modes, and post and pre-address update modes with variable offsets.

### Cache Configuration:

- Direct mapped I-cache and cache controller with coderam supports algorithms handled on chip
- Local Load Store RAM. The Load Store RAM is a fast access single cycle data RAM which overlays a section of the main memory, so the data access need not go through the Memory Arbitration Unit and the Memory Sequencer to the external memory. It is like a local data cache and typically can be used as a stack accelerator.



## Development System

The Evaluation System provides a complete Residential Gateway Solution. A hardware block diagram of the Evaluation System is given in Figure 1. This board can support four channels voice interface. The interface to the network is through a 10BaseT Ethernet. Software configuration of the system is summarized in Figure 2. The MGCP protocol Network Stack are by Accelerated Technology (Nucleus).

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