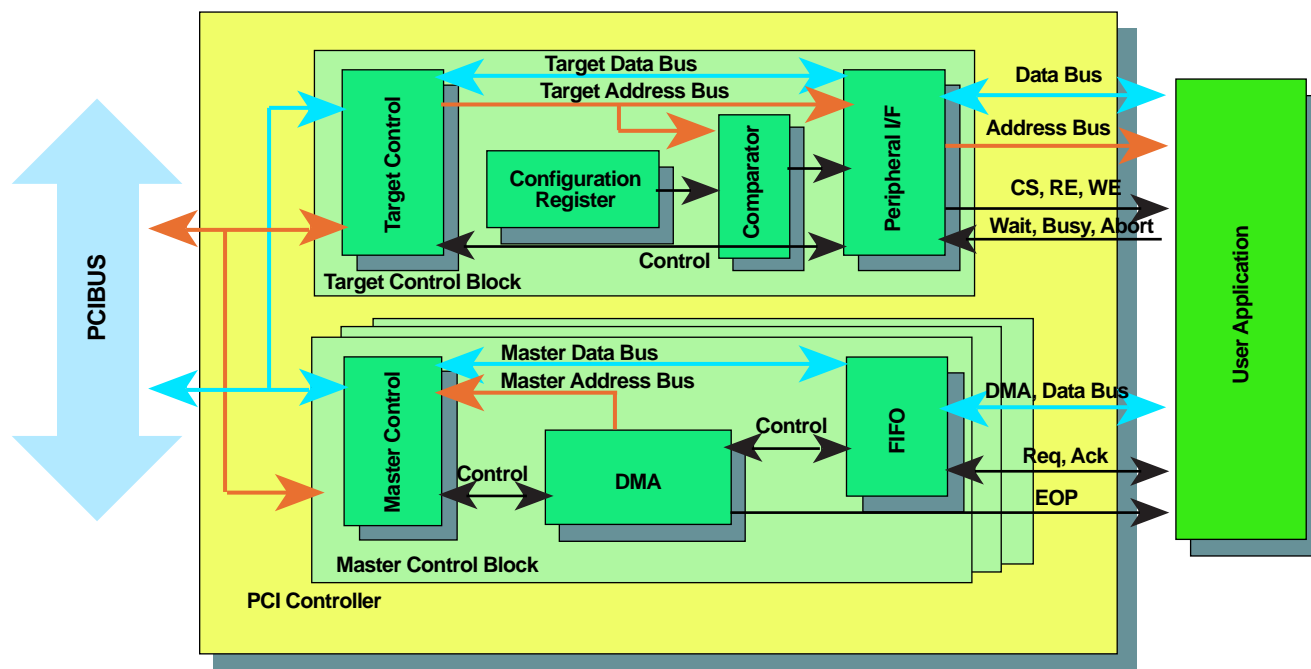


Standard Bus IP: PCI 2.2



Features

- Compliant to PCI Local Bus Specification Rev 2.2
- 33/66 MHz operations, 3.3V signalling level
- Available as target only, or target and master mode (1-3 masters)
- Compliant to Power Management Specification Rev 1.1
- Built-in master and target FIFO (bi-directional)
- Supports asynchronous operation (LCLK asynchronous mode)
- Supports no-wait burst transfer operation under master and target modes (up to 133MB/s at 33Hz and 266MB/s at 66MHz)
- Supports customization of configuration registers in CONFIG ROM block
- Supports delay target transactions
- PCI transceivers available in 0.18u, 0.25u and 0.35u processes for tighter ASIC integration (5V tolerant)
- ASIC library core within Fujitsu Design Flow

Overview

Fujitsu PCI core is RTL synthesizable module that provide interface between an application and PCI bus. All PCI protocol and timing requirements are handled by the macro. Various FIFO (both synchronous and asynchronous) depths can be configured. Macro support are target only (no FIFO), 1 target and 1-3 masters.

Both synchronous and asynchronous operations are supported. In asynchronous mode, PCI clock is running at different frequency from application clock. In synchronous operation, all signals to and from the application is synchronized with PCI clock.

The macro performs user setting using the internal ROM. It starts loading the ROM automatically after reset pin has been released. During ROM loading, it responds with 'Retry' to all PCI transactions, accepting PCI transactions after completion of loading.

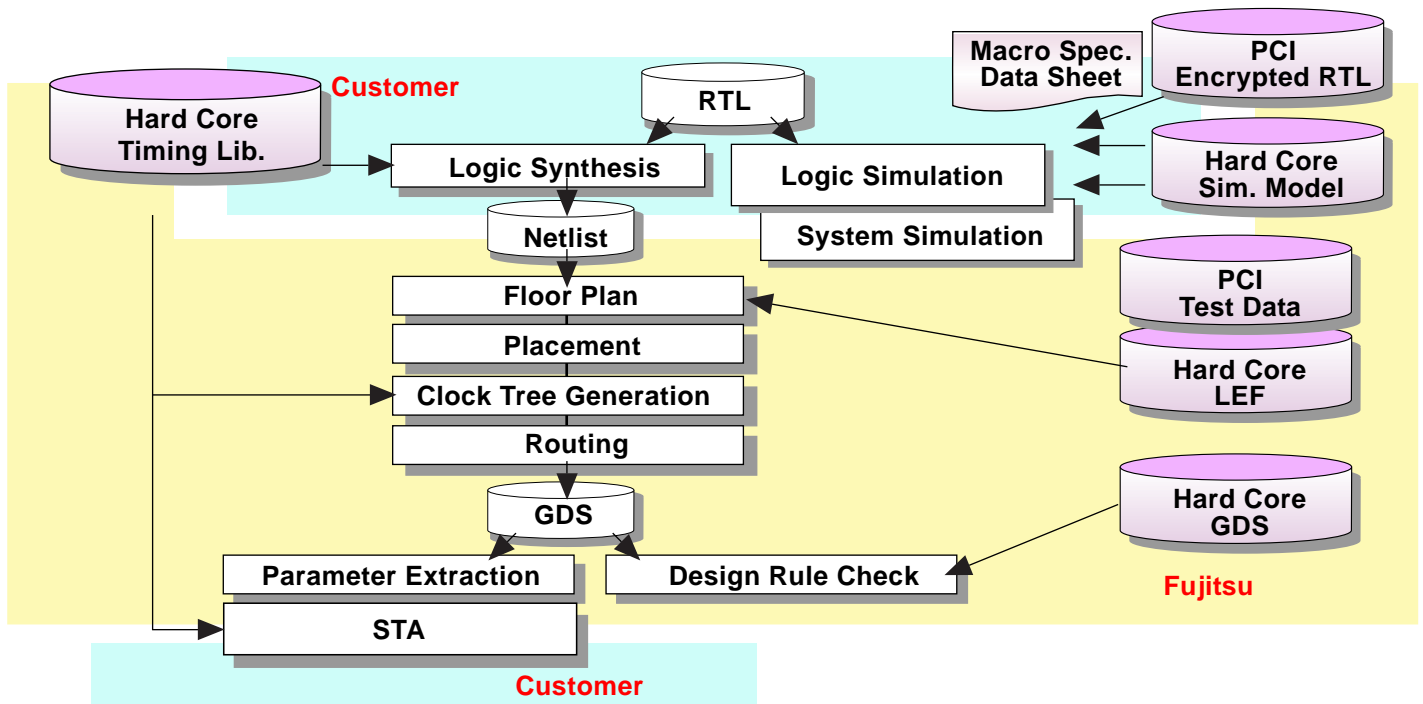
ASIC Development Support

Fujitsu provides analog macro to supplement ASIC development, such as PCI transceiver, and APLL (various speed combinations). We provide accurate timing model for ASIC simulation and Static Timing Analysis (STA). Soft core approach makes it easy to integrate into an ASIC.

Fujitsu provides a set of functional vectors to customer for final chip verification. Our application engineer will work with you on full chip Design for Testability (DfT) consultation.

Deliverables:

- Test chip for ASIC prototyping
- Test chip and macro specifications
- Encrypted RTL for top level simulation
- Application notes and testability guide
- Test benches for standalone IP verifications



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