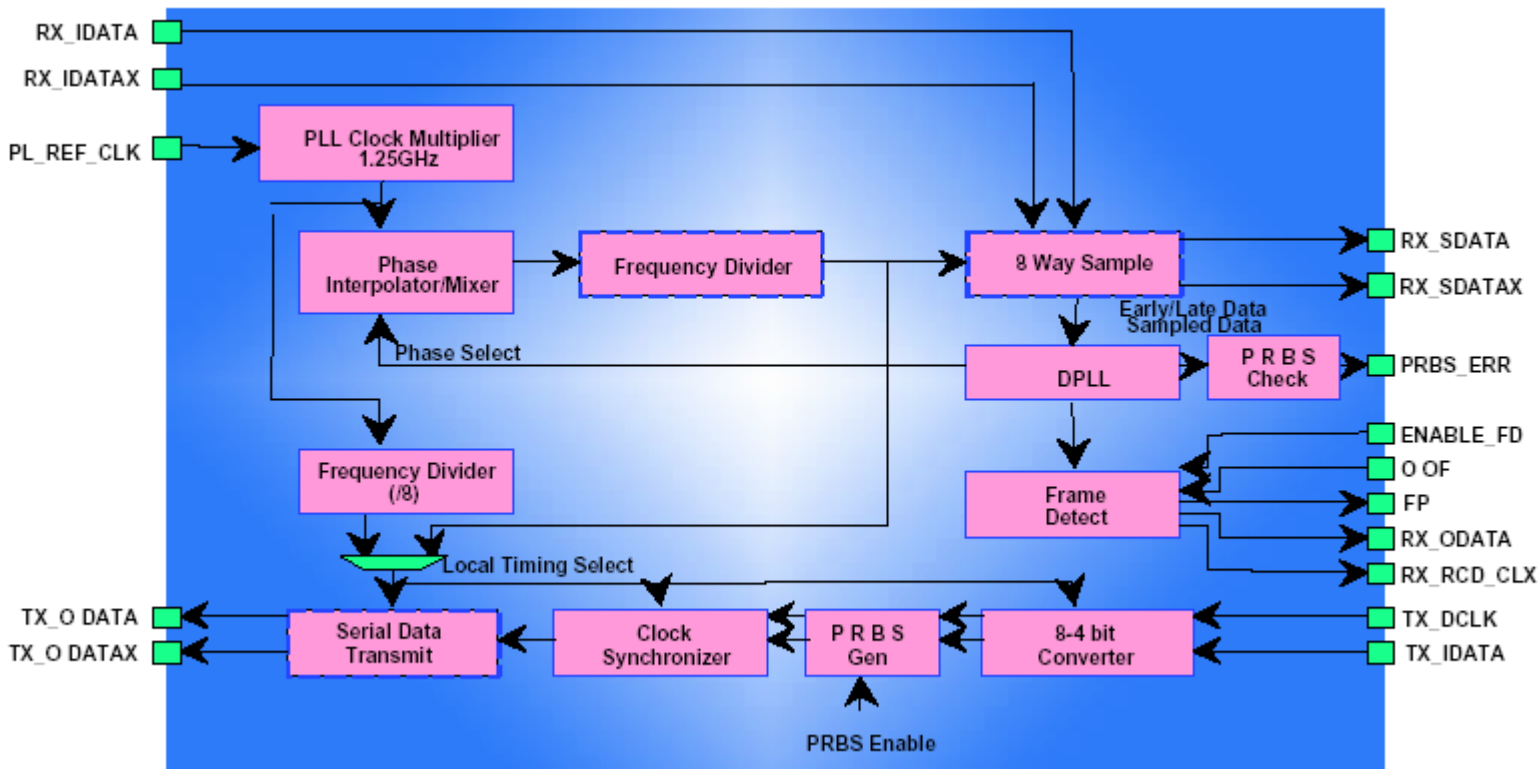


Networking and Communication IP: 622MHz with CDR



Features

- Compliant with ANSI, Bellcore and ITU-T Specifications (G825, G958 Type A)
- Clock and data recovery from 622/673 Mb/s data streams.
- Low recovered clock jitter
- Digital PLL
- LVDS interface for 622/673Mb/s connections.
- Serial-parallel and parallel-serial converters, frame detect (optional).
- Built-in self test (BIST) and Loopback for simplified production test
- Single and multiple channel hard macros available on request
- 0.18mm triple well CMOS process
- Macros qualified with various BGA packages
- Proven ASIC integration flow

Overview

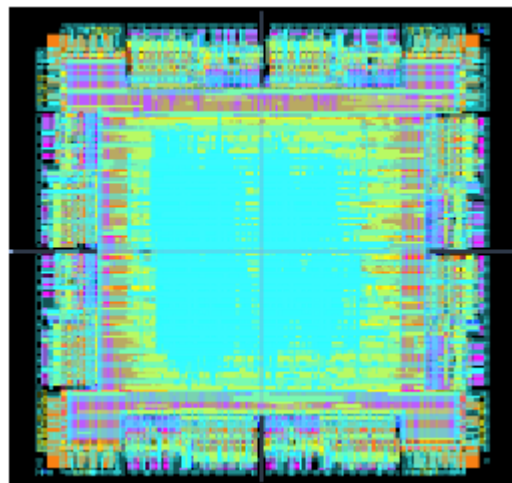
Fujitsu 622MHz CDR hard macro integrates both clock multiplier (APLL) and clock recovery circuitry (DPLL) for interfacing to 622/673Mb/s serial data stream. Parallel-serial and serial-parallel conversions are also performed with Frame detection (optional).

The macro has been designed to produce a low jitter recovered clock from the serial data stream with performance that exceeds the minimum tolerance for SDH/SONET network interfaces as

proposed by ITU-T specifications G825 and G958 Type A. BIST and internal Loopback modes are supported, which allow at speed functional self test, a powerful feature as it removes the need for the use of expensive Mixed Signal testing in production and hence is lower cost.

The CDR macro consists of a number the basic building blocks, Rx Channel (includes DPLL), Tx Channel, APLL. These building block can be assembled in a very flexible manner to meet customer specific requirements, for example.

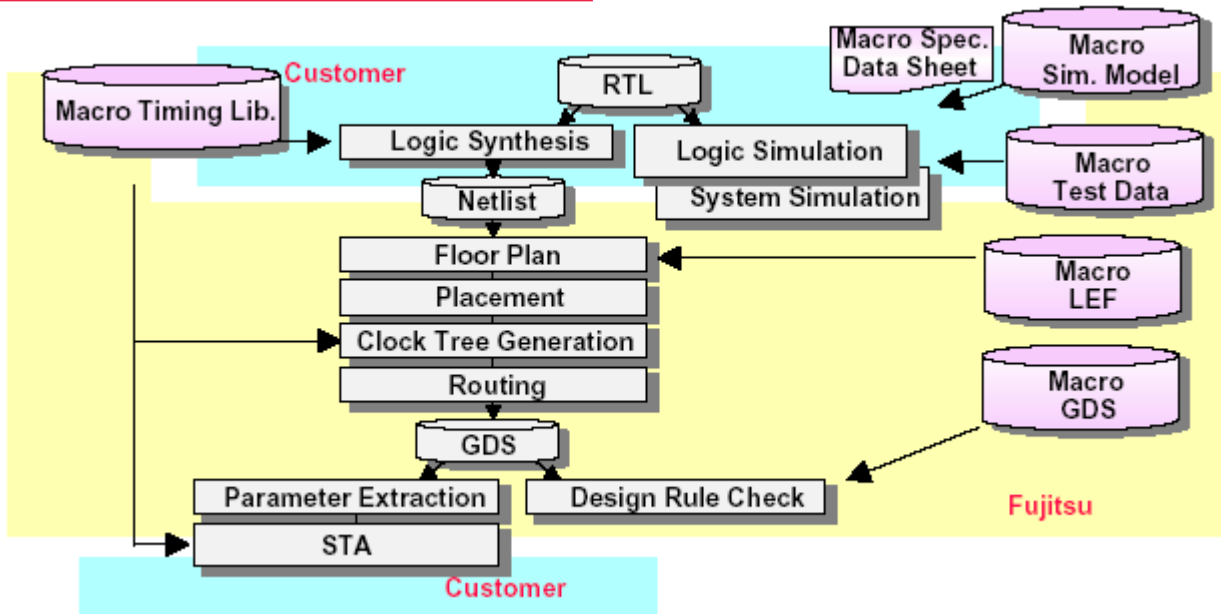
8 x Rx Channels, 8 x Tx Channels, double APLL 1 transmit and 1 receive.



Application example:

64 Channels of CDR, FCBGA Package.

ASIC Development Flow



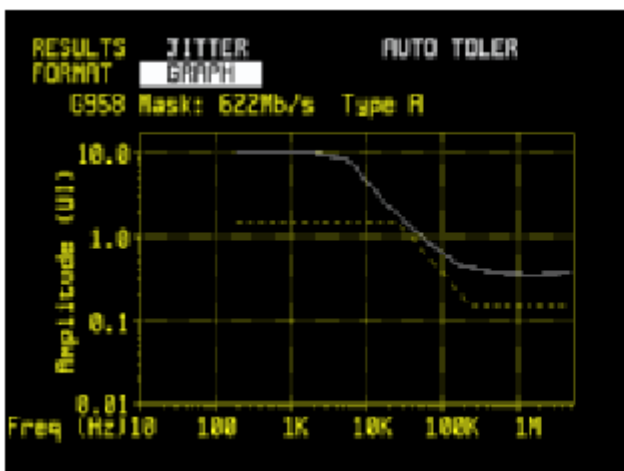
Fujitsu has established a robust ASIC design flow to integrate High Speed IO into customer ASICs. This methodology includes macro integration into layout, test verification, custom package design and signal integrity (SI) support. A single channel (Rx + Tx) CDR macro has been prototyped in an Evaluation Chip together with noise generation circuitry to mimic noisy ASIC environment due to extensive logic switching. The test chip was a qualification vehicle for the CDR macro. We then assemble each CDR macro to meet specific customer requirements - number of channels, type of package.

The CDR complete macro database (layout model, test model, timing model) is then handed over to the ASIC engineer for integration into the ASIC. As the CDR macro is a hard macro, macro timing is guaranteed, regardless of ASIC floor plan variations.

Maximum channels per macro is 8. Multiple macros are possible for application that requires higher channels.

Packages supported are PBGA, EBGA and FCBGA for various heat dissipation capability of overall ASIC.

SONET Test results



Point	Frequency	Mask(UI)	Tol(UI)	Result
1	200	1.50	>10.00	PASS
2	616	1.50	>10.00	PASS
3	1898	1.50	>10.00	PASS
4	5848	1.50	8.46	PASS
5	18016	1.50	2.64	PASS
6	55505	0.68	1.04	PASS
7	170998	0.22	0.50	PASS
8	526805	0.15	0.38	PASS
9	1622968	0.15	0.38	PASS
10	5000000	0.15	0.39	PASS

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