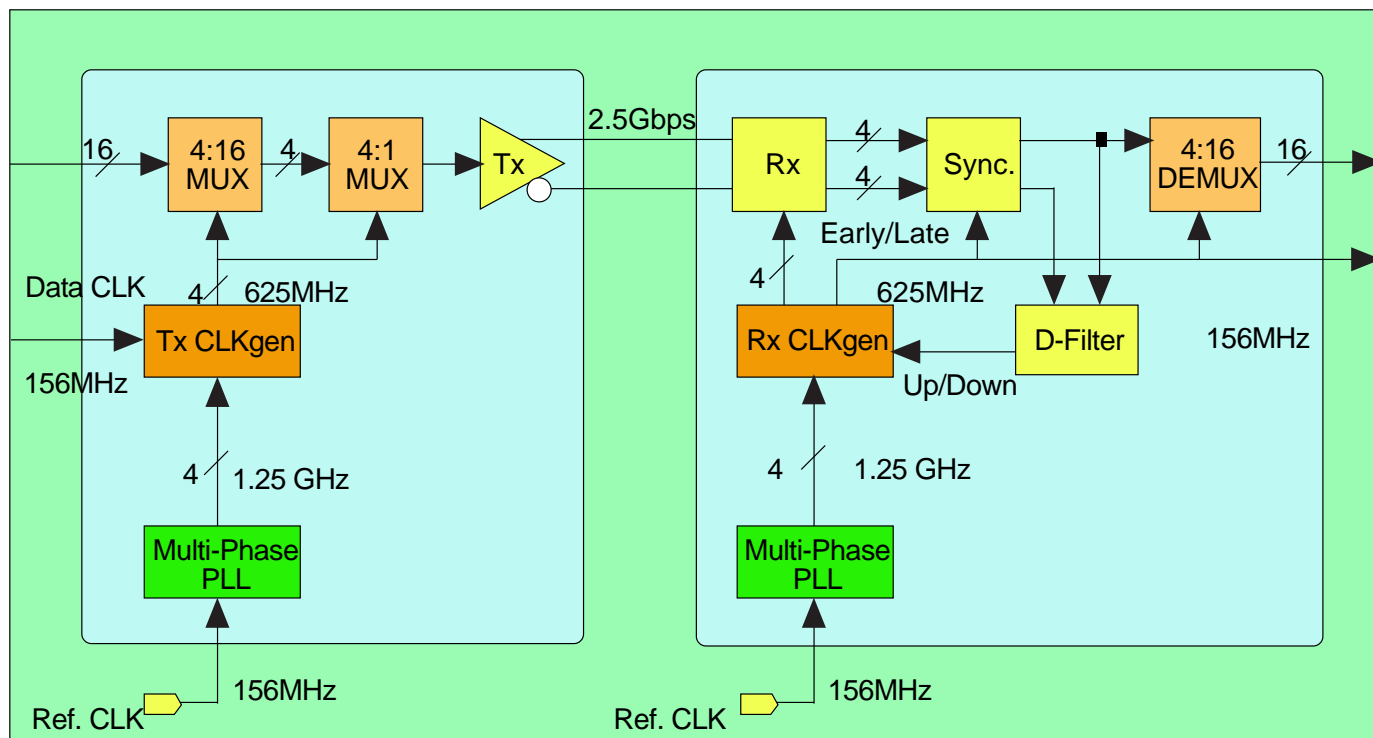


Networking and Communication IP: 2.5G with CDR



Features

- CMOS 0.18 micron technology
- 16-bit parallel transmitter and receiver arrays, other bit width also available
- Field programmable triple mode input data rate, 2.5Gbps, 1.25Gbps, and 622Mbps
- Differential PCML transmitter ($V_{t}=1.8V$)
- Equalized receiver obviating the need for pre-emphasis thereby reducing power dissipation
- 156MHz input reference clock
- Individual bit clock phase recovery using CDR (Clock Data Recovery)
- Complies with SONET/SDH jitter tolerance mask
- Integrated on-chip 50 ohm termination resistor on transmitter and receiver
- Field programmable transmitter output current control enabling optimum power consumption per application
- Low power < 2.5W for 16-bit transmitter array and 16-bit receiver array (typical)

Overview

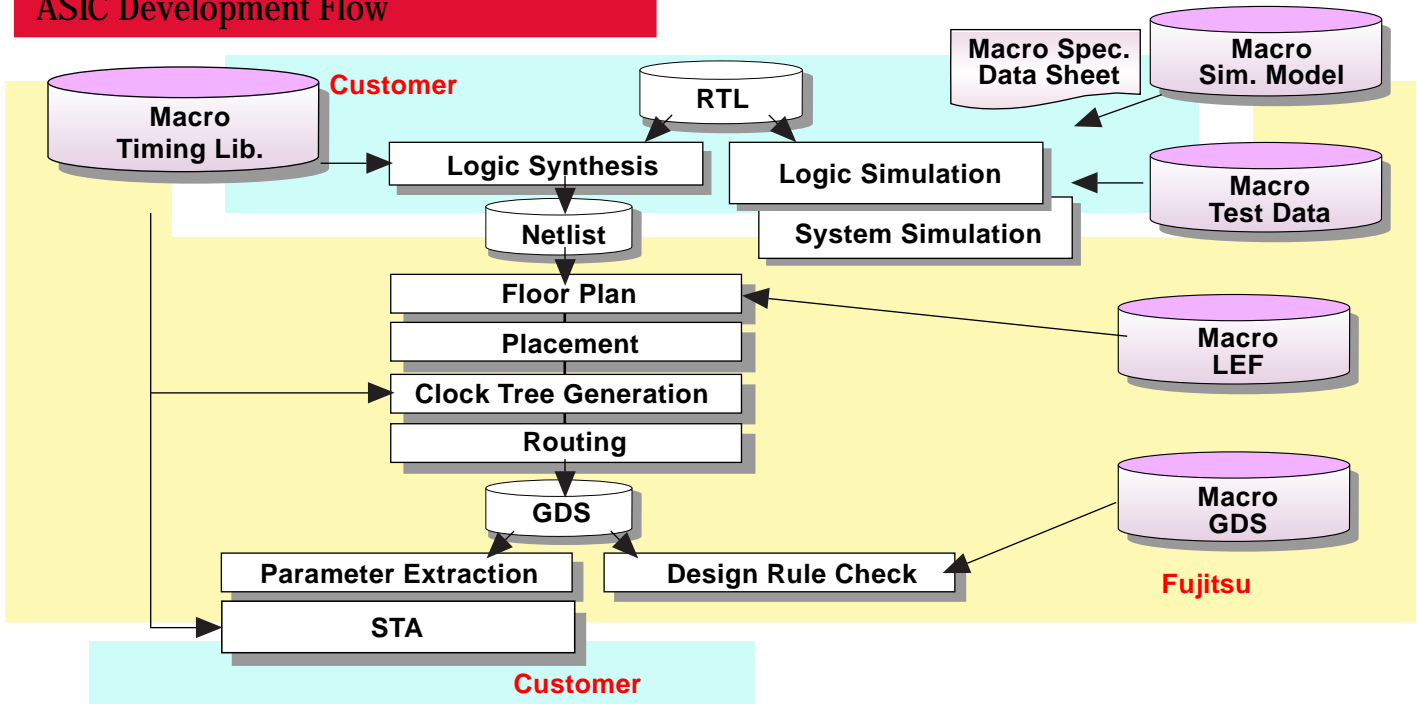
Fujitsu's triple mode parallel transceiver is a physical I/O interface macro for ASICs that performs high-speed back plane data communication, operating at low power dissipation. The triple data transfer rates, 2.5G/1.25G/622M bps, can be selected depending on the system requirements. The macro consists of a 16-bit transmitter, and a 16-bit receiver array. The receiver macro contains CDR (Clock Data Recovery) using dual loop PLL (analog and digital PLL), that complies with SONET/SDH jitter tolerance mask, up to 72-bit run length. The Receiver has an integrated line equalization capability to compensate for inter-symbol-interference (ISI), which enables a wide variation in data link length and range, from short PCB trace to long twisted pair cables connections. The device also includes on-chip PRBS generators and comparators for testability.

The macro is fabricated using Fujitsu's advanced 0.18m m CMOS technology with supply voltage of 1.8V and 3.3V. It can be used with a variety of packages, such as EBGA and FCBGA.

This macro can be used in a variety of applications:

- Wavelength Division Multiplex (WDM) equipment
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

ASIC Development Flow

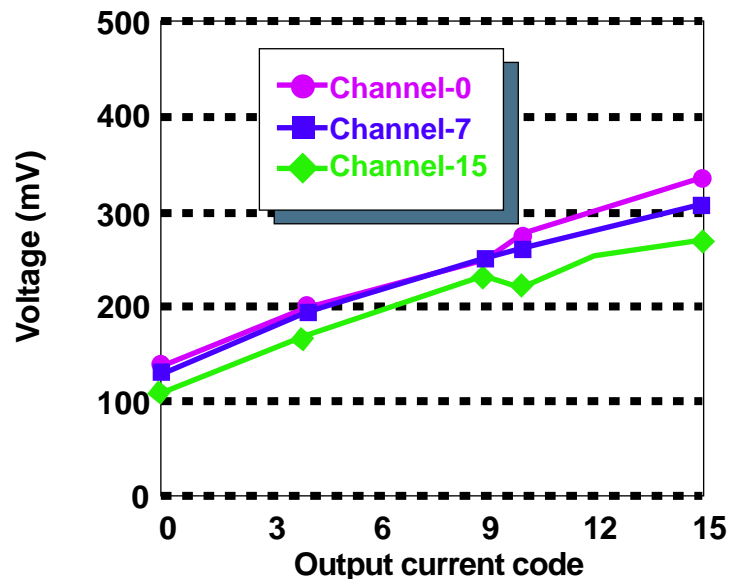
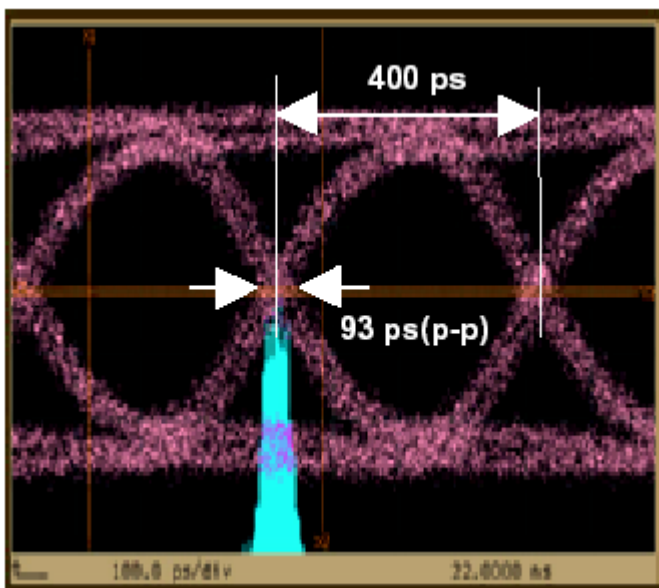


Fujitsu has established a robust ASIC design flow to integrate High Speed IO into customer ASIC. This methodology includes macro integration into layout, test verification, Custom package design and Signal Integration support.

We have proven the macro in testchip with noise generation circuitry to mimic noisy ASIC environment due to extensive logic switching.

We handcraft each macro to customer requirements in a single macro, ensuring consistent timing, regardless of ASIC floorplan variations. Maximum channel per macro is 16. Multiple macros are possible for application that requires higher channels. Packages supported are EBGA and FCBGA for various heat dissipation capability of overall ASIC.

Transmitter Evaluation Results



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