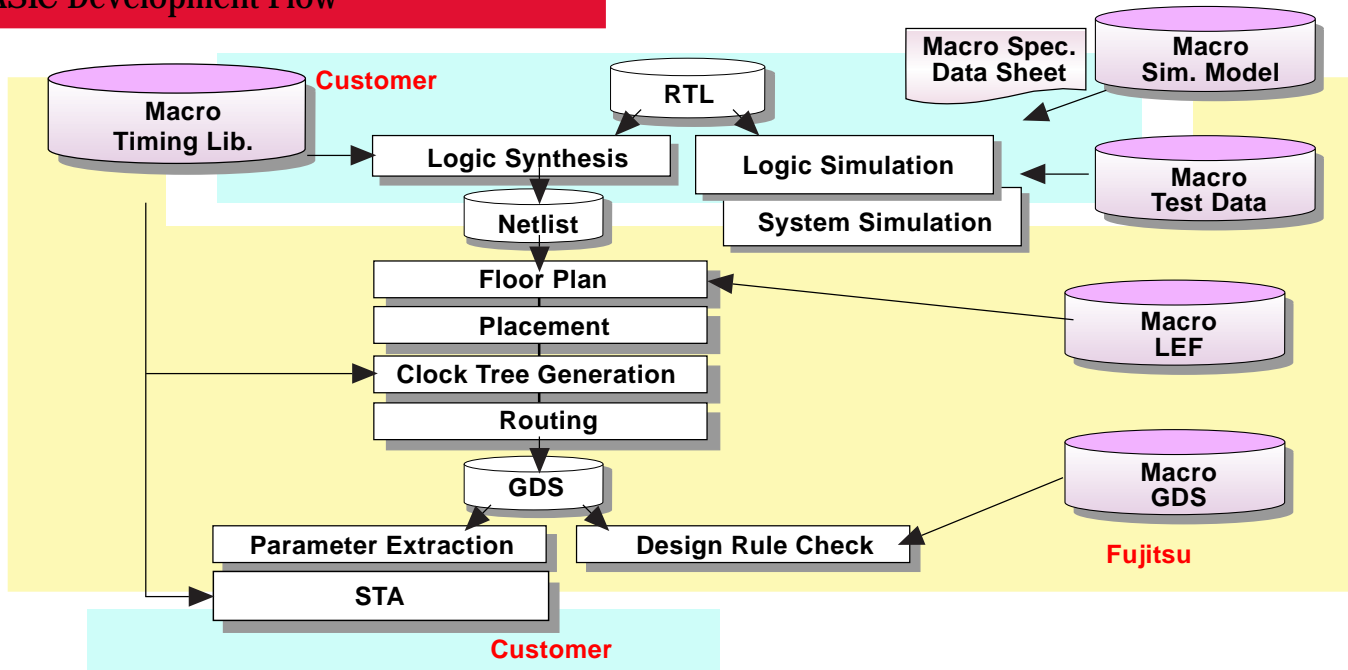


ASIC Development Flow



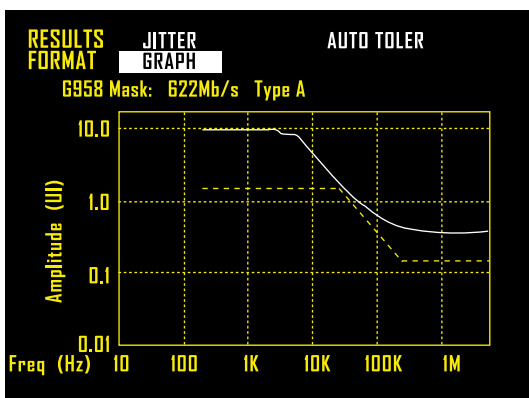
Fujitsu has established a robust ASIC design flow to integrate High Speed IO into customer ASICs. This methodology includes macro integration into layout, test verification, custom package design and signal Integrity (SI) support.

A single channel (Rx + Tx) CDR macro has been prototyped in an Evaluation Chip together with noise generation circuitry to mimic noisy ASIC environment due to extensive logic switching. The test chip was a qualification vehicle for the CDR macro. We then assemble each CDR macro to meet specific customer requirements - number of channels, type of package.

The CDR complete macro database (layout model, test model, timing model) is then handed over to the ASIC engineer for integration into the ASIC. As the CDR macro is a hard macro, macro timing is guaranteed, regardless of ASIC floor plan variations.

Maximum channels per macro is 8. Multiple macros are possible for application that requires higher channels. Packages supported are PBGA, EBGA and FCBGA for various heat dissipation capability of overall ASIC.

SONET Test results



RESULTS FORMAT	JITTER	PAGE	AUTO TOLER	
GRAPH	TEXT	1		
G958 Mask: 622Mb/s Type A				
Point	Frequency	Mask (UI)	Tol (UI)	Result
1	200	1.50	>10.00	PASS
2	616	1.50	>10.00	PASS
3	1898	1.50	>10.00	PASS
4	5848	1.50	8.46	PASS
5	18016	1.50	2.64	PASS
6	55505	0.68	1.04	PASS
7	170998	0.22	0.50	PASS
8	526805	0.15	0.38	PASS
9	1622968	0.15	0.38	PASS
10	5000000	0.15	0.39	PASS

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