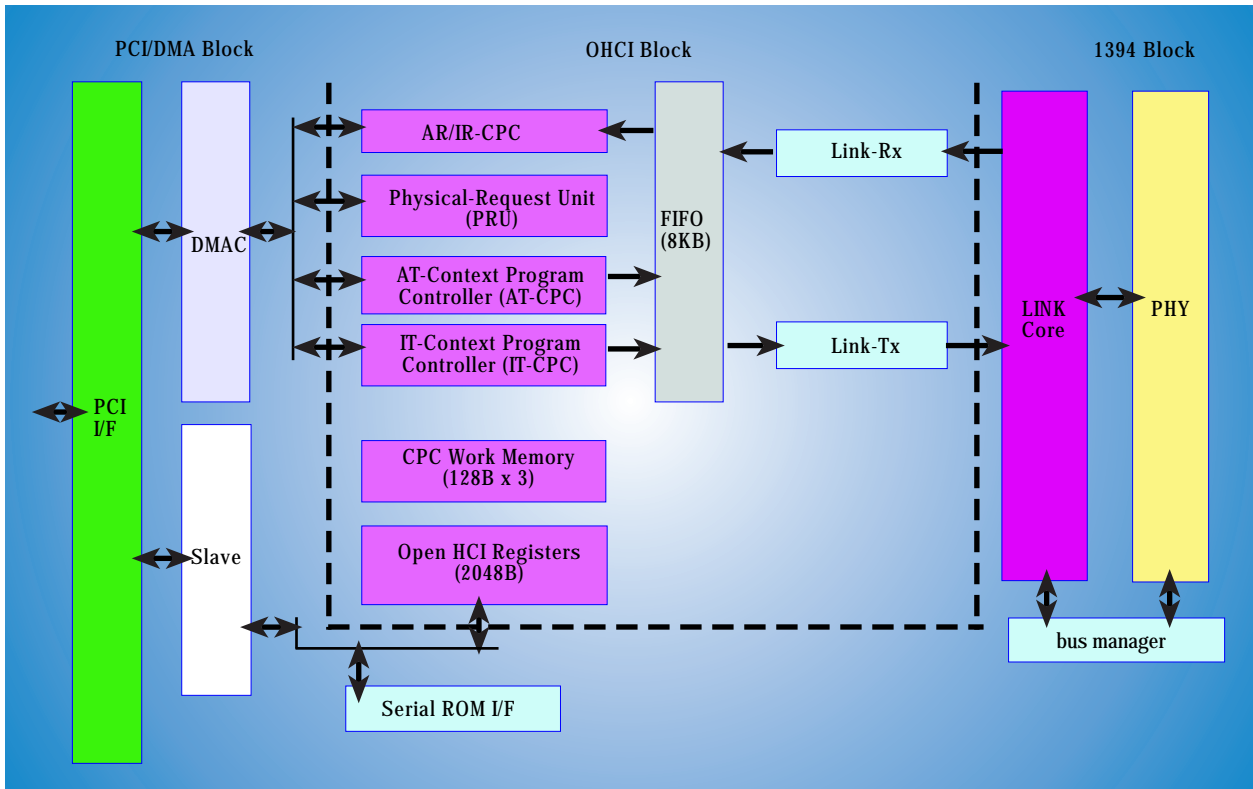


Standard Bus IP: IEEE1394 OHCI.1



Features

1394 Serial Bus Controller Block

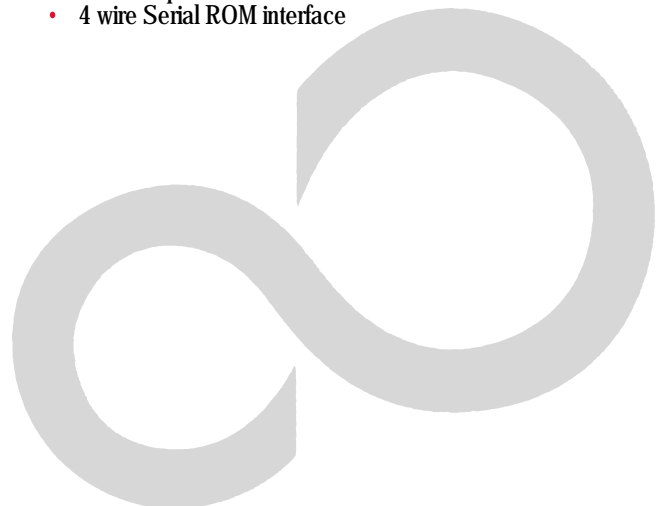
- Compliant with IEEE1394-1995 and 1394a-2000
- Integrated PHY and LINK layers
- 1394 port number : 1, 2 or 3 ports
- Transfer Data Rate : S100, S200, and S400
- Integrated APLL : 50MHz (LINK) and 400MHz (PHY)
- Cycle-Master Function
- On-chip Bus Management CSRs
- 6-pin cable supported
- On-chip transceiver and comparator
- On-chip comparator for detecting the cable power

Context Program Controller Block

- Compliant with Open HCI standard revision 1.1
- 13 independent ContextProgram Controllers
- 8 KB FIFO
- Context program work memory : 128B x 3

PCI Bus Controller Block

- Compliant with PCI local bus specification (revision 2.2)
- On-chip 32-bit DMA controller
- On-chip power management (PCI power management standard, revision 1.1, compliant)
- Alignment function
- Byte swap function
- 33MHz operation
- 4 wire Serial ROM interface



Overview

Fujitsu's IEEE1394-OHCI (Open Host Controller Interface) Controller Macro is compliant with IEEE1394-1995, 1394a-2000 and OHCI 1.1 specification.

Both LINK and PHY layers handles all 1394 protocols. PHY layers including analog PLL, transceiver, and comparator circuits. Customer can choose to integrate LINK only layer or LINK and PHY layers on ASIC for higher integration.

The PHY layer is designed in Fujitsu's unique triple well process. All analog circuits are isolated by the third well, drastically improve noise isolation.

In addition to the 1394 block, this macro contains various DMA engines called ContextProgram Controllers used for OHCI functions and PCI block. ContextProgram block consists of total 13 channels of independent DMA that are each dedicated to asynchronous and isochronous transmit and isochronous/asynchronous common receive operations.

Integrated PCI bus controller is compliant with PCI local bus standard (revision 2.2)

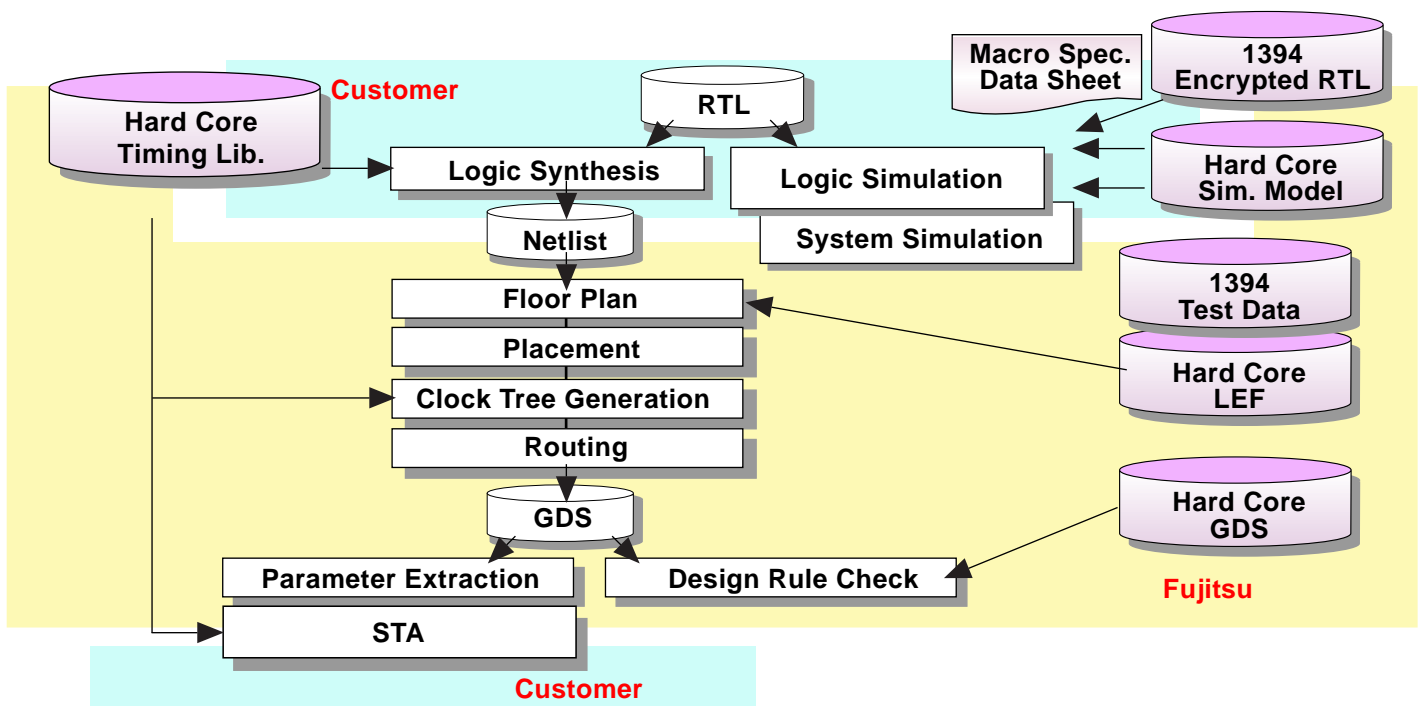
incorporating one 32-bit DMA controller and power management functions as specified in PCI bus power management specification (version 1.1).

ASIC Development Support

Fujitsu provide analog macro to supplement ASIC development, such as PHY layer, APLL (various speed combinations), and comparators. We also provide accurate timing model for ASIC synthesis, simulation and Static Timing Analysis (STA). Soft core approach makes it easy to integrate into overall ASIC. Fujitsu provides a complete set of functional vectors to customer for final chip verification. Our application engineer works closely with you to provide full chip Design for Test (DfT) consultation.

Deliverables:

- Evaluation board
- Evaluation board and macro specifications
- Encrypted RTL for top level simulation
- Application notes and testability guide
- Test benches for standalone IP verifications



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