ASSP for Power Management Applications of LCD Panel
4ch System Power Management IC for LCD Panel

MB39C313

■ DESCRIPTION
The MB39C313 is a 4ch system power management IC. It consists of 2-ch DC/DC Converter and 2-ch Charge pump. The DC/DC converter has excellent line regulation with the feed-forward method. Moreover, SW FET and phase compensator (Buck) is included, so that BOM can be reduced. It is most suitable for large size LCD panel power supply.

■ FEATURES
- Power supply voltage range: 8 V to 14 V
- For Buck Converter included SW FET (Vlogic): output 1.8 V to 3.3 V 1.5 A Max
- For Boost Converter included SW FET (Vs): output 18.1 V Max 1.5 A Max (at 12 V input and 15 V output)
- Negative Charge Pump with output voltage feedback (VGL): 50 mA Max
- Positive Charge Pump with output voltage feedback (VGH): 50 mA Max
- Error Amp threshold voltage: 1.213 V ± 1.5 % (Vlogic), 1.146 V ± 0.9 % (Vs), 0 V ± 36 mV (VGL), 1.213 V ± 2.1 % (VGH)
- Built-in soft-start circuit independent of loads
- Excellent line regulation by the feed-forward method (Vlogic, Vs)
- Built-in phase compensator parts (Vlogic)
- Built-in sequence comparator for rising
- Built-in short circuit protection (Vlogic)
- Built-in over voltage protection (Vs)
- Built-in over current protection (Vlogic, Vs)
- Built-in over temperature protection
- Frequency setting by input pin: 500 kHz / 750 kHz
- Package: TSSOP-28 Exposed PAD

■ APPLICATIONS
TFT LCD panels for LCD TV sets and monitors.
■ PIN ASSIGNMENT

(TOP VIEW)

- **FB**: 1, 28: SS
- **COMP**: 2, 27: GD
- **OS**: 3, 26: DLY2
- **SW**: 4, 25: DLY1
- **SW**: 5, 24: REF
- **PGND**: 6, 23: GND
- **PGND**: 7, 22: AVIN
- **SUP**: 8, 21: VINB
- **EN2**: 9, 20: VINB
- **DRP**: 10, 19: NC
- **DRN**: 11, 18: SWB
- **FREQ**: 12, 17: BOOT
- **FBN**: 13, 16: EN1
- **FBP**: 14, 15: FBB

(FPT-28P-M20)
### PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Block</th>
<th>Pin No.</th>
<th>Pin name</th>
<th>I/O</th>
<th>Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vlogic (Buck Converter)</strong></td>
<td>15</td>
<td>FBB</td>
<td>I</td>
<td>Vlogic Error Amp input pin</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>BOOT</td>
<td>—</td>
<td>Boot strap capacitor connection pin</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>SWB</td>
<td>O</td>
<td>Vlogic inductor connection pin</td>
</tr>
<tr>
<td>1</td>
<td>FB</td>
<td>I</td>
<td>Vs Error Amp input pin</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>COMP</td>
<td>O</td>
<td>Vs Error Amp output pin</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>SS</td>
<td>—</td>
<td>Vs Soft-start capacitor connection pin</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SW</td>
<td>I</td>
<td>Vs Inductor connection pin</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>SW</td>
<td></td>
<td>Vs Synchronous rectifier FET output pin</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>OS</td>
<td>O</td>
<td>Vs External SW drive output pin (NMOS open drain output)</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>GD</td>
<td>O</td>
<td>VGL external flying capacitor connection pin</td>
<td></td>
</tr>
<tr>
<td><strong>VGL (Negative Charge Pump)</strong></td>
<td>11</td>
<td>DRN</td>
<td>O</td>
<td>VGL external flying capacitor connection pin</td>
</tr>
<tr>
<td></td>
<td>13</td>
<td>FBN</td>
<td>I</td>
<td>VGL Error Amp input pin</td>
</tr>
<tr>
<td><strong>VGH (Positive Charge Pump)</strong></td>
<td>10</td>
<td>DRP</td>
<td>O</td>
<td>VGL external flying capacitor connection pin</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>FBP</td>
<td>I</td>
<td>VGH Error Amp input pin</td>
</tr>
<tr>
<td>16</td>
<td>EN1</td>
<td>I</td>
<td>Vlogic, VGL control pin</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>EN2</td>
<td>I</td>
<td>Vs, VGH control pin</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>FREQ</td>
<td>I</td>
<td>Frequency set pin “L”: 500 kHz, “H”: 750 kHz</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>DLY1</td>
<td>—</td>
<td>VGL start time setting capacitor connection pin</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>DLY2</td>
<td>—</td>
<td>Vs, VGH start time setting capacitor connection pin</td>
<td></td>
</tr>
<tr>
<td><strong>Control</strong></td>
<td>22</td>
<td>AVIN</td>
<td>—</td>
<td>Power supply pin</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>VINB</td>
<td>—</td>
<td>Vlogic Power supply pin</td>
</tr>
<tr>
<td></td>
<td>21</td>
<td>VINB</td>
<td>—</td>
<td>Vlogic Power supply pin</td>
</tr>
<tr>
<td>8</td>
<td>SUP</td>
<td>—</td>
<td>VGH Power supply pin</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>REF</td>
<td>O</td>
<td>Reference voltage output pin</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PGND</td>
<td>—</td>
<td>Drive block ground pin</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PGND</td>
<td>—</td>
<td>Drive block ground pin</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>GND</td>
<td>—</td>
<td>Ground pin</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>NC</td>
<td>—</td>
<td>Non connection pin</td>
<td></td>
</tr>
</tbody>
</table>
I/O PIN EQUIVALENT CIRCUIT DIAGRAM

<Error Amplifier (Boost Converter)>
Internal Supply (4.0 V)

FB 1

GND

<Error Amplifier Output for Compensation (Boost Converter)>
Internal Supply (4.0 V)

COMP 2

OS (19.8 V max.)

PGND

<Soft-start (Boost Converter)>
Internal Supply (4.0 V)

SS 28

GND

<Power-good (Boost Converter)>
OS (19.8 V max.)

GD 27

<Delay Control (Common)>
Internal Supply (4.0 V)

DLY2 26

GND

<Delay Control (Common)>
Internal Supply (4.0 V)

DLY1 25

GND

(Continued)
(Continued)

- **Switching Output (Negative Charge Pump)**
  - AVIN
  - DRN
  - PGND

- **Frequency Selection (Common)**
  - AVIN
  - FREQ
  - GND

- **Enable Control (Common)**
  - AVIN
  - EN1
  - GND

- **Error Amplifier (Negative Charge Pump)**
  - Internal Supply (4.0 V)
  - FBN
  - GND

- **Error Amplifier (Positive Charge Pump)**
  - Internal Supply (4.0 V)
  - FBP
  - GND

- **Boot Strap (Buck Converter)**
  - GND

- **Error Amplifier (Buck Converter)**
  - Internal Supply (4.0 V)
  - FBB
  - GND
FUNCTIONAL DESCRIPTIONS

V_logic : Buck Converter

The Buck converter is a fixed frequency PWM control asynchronous converter with integrated NMOS power switch. It features voltage mode control with input feed forward to improve line regulation performance. The converter is internally compensated and is designed to work with ceramic output capacitor. The main switch of the converter is a 3.2 A rated power NMOS with gate drive circuit reference to SWB pin (source terminal of the NMOS power FET). The gate drive circuit is powered from an internal 4 V regulator and is bootstrapped from SWB pin via an external capacitor to achieve driving capability beyond the supply rail.

Soft Start (Buck Converter)

The Buck converter has build in soft start control to limit the inrush current at start up. The soft start cycle start after EN1 is asserted and the duration is internally set to 1 ms. During the soft start cycle, the second non-inverting input of the error amplifier, refer to the block diagram, ramps up from 0 V. Thus, the Buck converter output ramps up in a control manner. The soft start cycle ends when the voltage on the second non-inverting input of the error amplifier rises above the reference voltage of 1.213 V.

Short Circuit Protection (Buck Converter)

The Buck converter is protected from short circuit fault by internal cycle-to-cycle current limit. In addition, the switching frequency is reduced to limit the power dissipation during the fault condition. The switching frequency reduction depends on the voltage on FBB pin. When the voltage of FBB pin is below 0.9 V and 0.6 V, the switching frequency reduces to 1/2 and 1/4 of the normal value respectively. The switching frequency becomes normal automatically if the normal situation was resumed.

Vs : Boost Converter

The Boost converter features fixed frequency pulse width modulated (PWM) control with integrated NMOS power switch. The switching frequency can be set to either 500 kHz or 750 kHz via the FREQ pin. The converter operates as an asynchronous Boost converter with external Schottky diode. The use of voltage mode control with input feed forward improves line regulation performance. In addition, the converter is designed with external frequency compensation that allows flexibility on selecting external component values. A PMOS switch with on resistance of 10 Ω connects between SW and OS pin so that it operates in parallel with the external Schottky diode. At high loading current, most of the inductor current flows through the external Schottky diode. At light load, the PMOS switch provides a conduction path that allows the inductor current flow in reverse direction. As a result, the converter stays in continuous conduction mode for most of the load current range and allows the use of simple frequency compensation scheme.

Soft Start (Boost Converter)

A build in soft start circuit with an external capacitor connects to SS pin provides soft start function for the Boost converter to prevent high inrush current during start up. The SS pin provides a constant charging current so that soft start time is adjustable by changing the capacitance value of an external capacitor. During start up, the output voltage of the Boost converter is controlled by the SS pin until the voltage on SS pin is higher than the voltage on FB pin and the soft start cycle ends.

Over Voltage Protection (Boost Converter)

The Boost converter has build in over voltage protection to prevent MB39C313 from being damaged due to excessive voltage stress under fault conditions such as FB pin is left floating or short to ground. The protection circuitry monitors the Boost converter output via OS pin and shut down the NMOS power FET that connects to SW pin when the voltage on OS pin is higher than 18.7 V. As a result, the inductor current start to fall and the output of the Boost converter follows. The Boost converter resumes normal operation when the voltage at OS pin falls below the protection threshold.
Gate Drive Pin (GD)

GD pin is an open drain output that triggers (pulls “Low”) after DLY2 expires and the voltage at FB pin rise above 1.03 V (90 % of FB reference voltage, 1.146 V). 1.03 V at FB pin translates to 90 % of the regulation point of the Boost converter. GD pin remains “Low” until the input voltage or voltage on EN2 is cycled to ground.

VGL : Negative Charge Pump

The negative charge pump uses fixed switching frequency regulated architecture. The output voltage is set externally by a resistor divider. The regulation is done by controlling the pump current in the driver. Refer to the system block diagram, the charge pump use external diodes, pumping capacitor and output filter capacitor. Since the input of the charge pump and the driver is connected to the supply pin (VIN), the maximum negative output voltage is -VIN + V.loss. V.loss includes voltage drop in external diodes and gate driver. Additional charge pump stage can be added to generate larger negative voltage.

VGH : Positive Charge Pump

The positive charge pump uses fixed switching frequency regulated architecture. The output voltage is set externally by a resistor divider. The regulation is done by controlling the pump current in the driver.

Refer to the system block diagram, the charge pump use external diodes, pumping capacitor and output filter capacitor. The input of the charge pump is connected to the Vs (Boost converter output) and the pump capacitor is charged to Vs during charging phase. As the supply to the driver (SUP pin) can be either the Vs (Boost converter output) or the VIN (supply PIN) of MB39C313, the maximum output voltage is V_SUP + Vs. Additional charge pump stage can be added to increase the maximum output voltage.

Common Block

Under Voltage Lockout

MB39C313 will shutdown when the supply voltage below 6 V to prevent improper operation of the device.

Over Temperature Protection

When the junction temperature rises above 150 °C, most of the active circuitries are shutdown to prevent damage from excessive power dissipation beyond safety limits.
Power Up Sequencing (EN1, EN2, DLY1, DLY2)

EN1 and EN2 pin control the power up sequence of MB39C313. The timing of the sequencing events is controlled by the capacitance on DLY1 and DLY2 pins. By pulling EN1 high, the Buck converter enables first. Then, the Negative Charge Pump is enabled after some delay time, DLY1. Pulling EN2 high, the Boost converter and Positive Charge Pump are enabled at the same time with some time delay, DLY2. If EN2 pin is pulled high when the Buck converter is already operating, the time delay DLY2 starts at the EN2 rising edge, Figure 1. Setting such delay time can be particularly useful if EN2 is already connected to input voltage (VIN). If EN2 is pulled high before the Buck converter is operating, the time delay DLY2 starts after the Buck converter is fully on, Figure 2.

- Figure 1. Power-On sequence with EN2 is always high

- Figure 2. Power-On sequence with EN1 and EN2 enabled separately
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>VDD</td>
<td>AVIN,VINB pin</td>
<td>−0.3</td>
<td>+17</td>
</tr>
<tr>
<td></td>
<td>VBOOT</td>
<td>BOOT pin</td>
<td>−0.3</td>
<td>+19.8</td>
</tr>
<tr>
<td></td>
<td>VSUP</td>
<td>SUP pin</td>
<td>−0.3</td>
<td>+19.8</td>
</tr>
<tr>
<td>Input voltage</td>
<td>VFB</td>
<td>FB, FBB, FBN, FBP pin</td>
<td>−0.3</td>
<td>+7</td>
</tr>
<tr>
<td></td>
<td>VDS</td>
<td>OS pin</td>
<td>−0.3</td>
<td>+19.8</td>
</tr>
<tr>
<td></td>
<td>VGD</td>
<td>GD pin</td>
<td>−0.3</td>
<td>+19.8</td>
</tr>
<tr>
<td></td>
<td>VEN</td>
<td>EN1,EN2 pin</td>
<td>−0.3</td>
<td>+17</td>
</tr>
<tr>
<td></td>
<td>VFREQ</td>
<td>FREQ pin</td>
<td>−0.3</td>
<td>+17</td>
</tr>
<tr>
<td>SW Voltage</td>
<td>VSWB</td>
<td>SWB pin</td>
<td>−0.7</td>
<td>+17</td>
</tr>
<tr>
<td></td>
<td>VSW</td>
<td>SW pin</td>
<td>−0.3</td>
<td>+19.8</td>
</tr>
<tr>
<td>SW peak current</td>
<td>I_SWB</td>
<td>SWB pin AC</td>
<td>—</td>
<td>3.9</td>
</tr>
<tr>
<td></td>
<td>I_SW</td>
<td>SW pin AC</td>
<td>—</td>
<td>4.2</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>P_D</td>
<td>Ta ≤ +25 °C</td>
<td>—</td>
<td>3.44*</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>T_STG</td>
<td>—</td>
<td>−55</td>
<td>+125</td>
</tr>
</tbody>
</table>

* : When mounted on a 100mm × 100 mm: 4 layer.

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.
## RECOMMENDED OPERATION CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>VDD, VBOOT, VSUP</td>
<td>AVIN, VINB pin, BOOT pin, SUP pin</td>
<td>8, 13, 8.0</td>
<td>12, 17, 12.0</td>
</tr>
<tr>
<td>REF pin output current</td>
<td>IREF</td>
<td>REF pin</td>
<td>−50</td>
<td>−0</td>
</tr>
<tr>
<td>Input voltage</td>
<td>VFB, VOS</td>
<td>FB, FBB, FBN, FBP pin, OS pin</td>
<td>0, 0</td>
<td>5.5, 18.1</td>
</tr>
<tr>
<td>Output voltage</td>
<td>V0</td>
<td>Vlogic: Buck Converter</td>
<td>1.8</td>
<td>3.3</td>
</tr>
<tr>
<td>Output current</td>
<td>I0</td>
<td>Vlogic: Buck Converter DC</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>BOOT pin capacitor</td>
<td>CBOOT</td>
<td>BOOT pin</td>
<td>0.01</td>
<td>1.00</td>
</tr>
<tr>
<td>REF pin capacitor</td>
<td>CREF</td>
<td>REF pin</td>
<td>0.10</td>
<td>0.22</td>
</tr>
<tr>
<td>DRP, DRN pin capacitor</td>
<td>CDRP</td>
<td>DRP, DRN pin</td>
<td>0.10</td>
<td>0.47</td>
</tr>
<tr>
<td>SS pin capacitor</td>
<td>CSS</td>
<td>SS pin</td>
<td>—</td>
<td>0.022</td>
</tr>
<tr>
<td>DLY pin capacitor</td>
<td>CDLY</td>
<td>DLY1, DLY2 pin</td>
<td>—</td>
<td>0.01</td>
</tr>
<tr>
<td>Vlogic output filter capacitor</td>
<td>Cout</td>
<td>Vlogic: Buck Converter</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>Vs output filter capacitor</td>
<td>Cout</td>
<td>Vs: Boost Converter</td>
<td>—</td>
<td>66</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>Ta</td>
<td></td>
<td>−30</td>
<td>+25, +85</td>
</tr>
</tbody>
</table>

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Pin No.</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Voltage Block [VREF]</td>
<td>Output voltage</td>
<td>VREF</td>
<td>24</td>
<td>REF = 0 mA</td>
<td>Min</td>
</tr>
<tr>
<td>Bias Voltage Block [VB]</td>
<td>Output voltage</td>
<td>VB</td>
<td>17</td>
<td>BOOT = -1 mA, BOOT pin</td>
<td>3.5</td>
</tr>
<tr>
<td>Under Voltage Lockout Protection Circuit Block [UVLO]</td>
<td>Threshold voltage</td>
<td>VTLH</td>
<td>22</td>
<td>AVIN = ( \tilde{V} )</td>
<td>5.6</td>
</tr>
<tr>
<td></td>
<td>Hysteresis width</td>
<td>VH</td>
<td>22</td>
<td>—</td>
<td>0.2*</td>
</tr>
<tr>
<td>Over Temperature Protection Block [OTP]</td>
<td>Stop temperature</td>
<td>TOTPH</td>
<td>—</td>
<td>T junction</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Hysteresis width</td>
<td>TOTPHYS</td>
<td>—</td>
<td>—</td>
<td>+ 15*</td>
</tr>
<tr>
<td>Oscillator Block [OSC]</td>
<td>Output frequency</td>
<td>fOSC</td>
<td>4, 5, 10, 11, 18</td>
<td>FREQ = &quot;H&quot;</td>
<td>600</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fOSC</td>
<td>4, 5, 10, 11, 18</td>
<td>FREQ = &quot;L&quot;</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td>Input voltage</td>
<td>VIH</td>
<td>12</td>
<td>fosc = 750 KHz set</td>
<td>1.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIL</td>
<td>12</td>
<td>fosc = 500 KHz set</td>
<td>—</td>
</tr>
<tr>
<td>Sequence Control Block [SEQ CTL]</td>
<td>Threshold voltage</td>
<td>VTH</td>
<td>25, 26</td>
<td>DLY1, DLY2 pin</td>
<td>1.123</td>
</tr>
<tr>
<td></td>
<td>Charging current</td>
<td>IDLY</td>
<td>25, 26</td>
<td>DLY1, DLY2 = 0 V</td>
<td>3.8</td>
</tr>
<tr>
<td>Control Block [CTL]</td>
<td>Input voltage</td>
<td>VIH</td>
<td>9, 16</td>
<td>EN1, EN2 ON</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIL</td>
<td>9, 16</td>
<td>EN1, EN2 OFF</td>
<td>—</td>
</tr>
<tr>
<td>General</td>
<td>Stand by current</td>
<td>ICCS</td>
<td>22</td>
<td>EN1, EN2 = 0 V, AVIN pin</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ICCS</td>
<td>20, 21</td>
<td>EN1, EN2 = 0 V, VINB pin</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ICCS</td>
<td>8</td>
<td>EN1, EN2 = 0 V, SUP pin</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>Power supply current</td>
<td>ICC</td>
<td>22</td>
<td>EN1, EN2 = AVIN, AVIN pin</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ICC</td>
<td>20, 21</td>
<td>EN1, EN2 = AVIN, VINB pin</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ICC</td>
<td>8</td>
<td>EN1, EN2 = AVIN, SUP pin</td>
<td>—</td>
</tr>
</tbody>
</table>
### Parameter Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Pin No.</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage</td>
<td>$V_{TH}$</td>
<td>15</td>
<td>FBB pin</td>
<td>1.195</td>
<td>1.213</td>
<td>1.231</td>
<td>V</td>
</tr>
<tr>
<td>Input bias current</td>
<td>$I_b$</td>
<td>15</td>
<td>FBB = 0 V</td>
<td>-100</td>
<td>0</td>
<td>+100</td>
<td>nA</td>
</tr>
<tr>
<td>SW NMOS-Tr On resistor</td>
<td>$R_{ON}$</td>
<td>18, 20, 21</td>
<td>SWB = -500 mA VGS = 4 V</td>
<td>—</td>
<td>230*</td>
<td>—</td>
<td>mΩ</td>
</tr>
<tr>
<td>SW NMOS-Tr Leak current</td>
<td>$I_{LEAK}$</td>
<td>18, 20, 21</td>
<td>EN1 = 0 V SWB = 0 V</td>
<td>-10</td>
<td>—</td>
<td>—</td>
<td>μA</td>
</tr>
<tr>
<td>Over current protect</td>
<td>$I_{LIM}$</td>
<td>18</td>
<td>SWB pin</td>
<td>2.5</td>
<td>3.2</td>
<td>3.9</td>
<td>A</td>
</tr>
<tr>
<td>Short circuit protect threshold voltage</td>
<td>$V_{TH}$</td>
<td>15</td>
<td>$f_{OSC} \times 1/2$</td>
<td>0.855</td>
<td>0.900</td>
<td>0.945</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{TH}$</td>
<td>15</td>
<td>$f_{OSC} \times 1/4$</td>
<td>0.57</td>
<td>0.60</td>
<td>0.63</td>
<td>V</td>
</tr>
<tr>
<td>Soft-start time</td>
<td>tss</td>
<td>15</td>
<td>FBB pin</td>
<td>0.69</td>
<td>1.00</td>
<td>1.50</td>
<td>ms</td>
</tr>
</tbody>
</table>

(Continued)
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Pin No.</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Min</td>
<td>Typ</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>( V_{TH} )</td>
<td>1</td>
<td>FB pin</td>
<td>1.136</td>
<td>1.146</td>
</tr>
<tr>
<td>Input bias current</td>
<td>( I_b )</td>
<td>1</td>
<td>FB = 0 V</td>
<td>-100</td>
<td>0</td>
</tr>
<tr>
<td>SW NMOS-Tr On resistor</td>
<td>( R_{ON} )</td>
<td>4,5</td>
<td>SW = 500 mA ( V_{GS} = 5 ) V</td>
<td>—</td>
<td>110*</td>
</tr>
<tr>
<td>SW PMOS-Tr On resistor</td>
<td>( R_{ON} )</td>
<td>3,4,5</td>
<td>OS = -200 mA ( V_{GS} = 12 ) V</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>SW NMOS-Tr Leak current</td>
<td>( I_{LEAK} )</td>
<td>4,5</td>
<td>EN2 = 0 V OS = 15 V SW = 0 V</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>SW PMOS-Tr Leak current</td>
<td>( I_{LEAK} )</td>
<td>3</td>
<td>EN2 = 0 V SW = 15 V</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>Over current protect</td>
<td>( I_{LIM} )</td>
<td>4,5</td>
<td>SW pin</td>
<td>2.8</td>
<td>3.5</td>
</tr>
<tr>
<td>Over voltage protect</td>
<td>( V_{OVP} )</td>
<td>3</td>
<td>OS = ( \frac{1}{3} )</td>
<td>18.5</td>
<td>18.7</td>
</tr>
<tr>
<td>Soft-start charging current</td>
<td>( I_{SS} )</td>
<td>28</td>
<td>SS = 0 V</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>GD Threshold voltage</td>
<td>( V_{TH} )</td>
<td>1</td>
<td>FB = ( \frac{1}{3} )</td>
<td>1.01</td>
<td>1.03</td>
</tr>
<tr>
<td>GD “L” level output voltage</td>
<td>( V_{OL} )</td>
<td>27</td>
<td>GD = 500 μA</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>GD output leak current</td>
<td>( I_{LEAK} )</td>
<td>27</td>
<td>GD = 17 V</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

### Vs [Boost Converter]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Pin No.</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O voltage difference</td>
<td>( V_{drop} )</td>
<td>11</td>
<td>DRN = 50 mA FBP = nominal-5%</td>
<td>—</td>
<td>130</td>
</tr>
<tr>
<td>VGL [Negative Charge Pump]</td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>270</td>
</tr>
</tbody>
</table>

(Continued)
### MB39C313

(Continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Pin No.</th>
<th>Condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold voltage</td>
<td>V&lt;sub&gt;TH&lt;/sub&gt;</td>
<td>14</td>
<td></td>
<td>1.187</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.213</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.238</td>
<td></td>
</tr>
<tr>
<td>Input bias current</td>
<td>I&lt;sub&gt;B&lt;/sub&gt;</td>
<td>14</td>
<td>FBP = 0 V</td>
<td>-100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>+100</td>
<td></td>
</tr>
<tr>
<td>On resistor</td>
<td>R&lt;sub&gt;ON&lt;/sub&gt;</td>
<td>10</td>
<td>I&lt;sub&gt;out&lt;/sub&gt; = 20 mA</td>
<td>—</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.65</td>
<td></td>
</tr>
<tr>
<td>I/O voltage difference</td>
<td>V&lt;sub&gt;drop&lt;/sub&gt;</td>
<td>10</td>
<td>V&lt;sub&gt;drop&lt;/sub&gt; = SUP-DRP</td>
<td>—</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DRP = -50 mA</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FBP = nominal-5%</td>
<td>680</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>850</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1600</td>
<td></td>
</tr>
</tbody>
</table>

* : This parameter isn't be specified. This should be used as a reference to support designing the circuit
TYPICAL CHARACTERISTICS

Threshold voltage vs. Operating Ambient Temperature

Switching Frequency vs. Operating Ambient Temperature

REF vs. Operating Ambient Temperature

RON Resistance vs. Operating Ambient Temperature

RON Resistance vs. Operating Ambient Temperature

RON Resistance vs. Operating Ambient Temperature

(Continued)
(Continued)

### Power dissipation vs. Operating ambient temperature

<table>
<thead>
<tr>
<th>Power dissipation $P_D$ (mW)</th>
<th>Operating ambient temperature $T_a$ (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3500</td>
<td>-40</td>
</tr>
<tr>
<td>3440</td>
<td>-30</td>
</tr>
<tr>
<td>3000</td>
<td>-20</td>
</tr>
<tr>
<td>2500</td>
<td>0</td>
</tr>
<tr>
<td>2000</td>
<td>+20</td>
</tr>
<tr>
<td>1500</td>
<td>+40</td>
</tr>
<tr>
<td>1000</td>
<td>+60</td>
</tr>
<tr>
<td>500</td>
<td>+80</td>
</tr>
<tr>
<td>0</td>
<td>+100</td>
</tr>
</tbody>
</table>

---

**Note:** The graph shows the relationship between power dissipation and operating ambient temperature. The data points are given in the table above.
### SET UP

1. **Setting Control Pin**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Channels</th>
<th>Standby</th>
<th>Operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN1</td>
<td>V\text{\textsubscript{LOGIC}}: Buck converter</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>V\text{\textsubscript{AL}}: Negative Charge Pump</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN2</td>
<td>V\text{\textsubscript{S}}: Boost converter</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td></td>
<td>V\text{\textsubscript{GH}}: Positive Charge Pump</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2. **Setting Switching Frequency**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Setting</th>
<th>Internal oscillator frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQ</td>
<td>H</td>
<td>750 kHz</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>500 kHz</td>
</tr>
</tbody>
</table>

3. **Protection Circuitry**

3.1) **IC**

Under voltage lock out: AVIN \leq 6 V, all channels shut down

3.2) **V\text{\textsubscript{LOGIC}}**: Buck Converter

Short circuit protection: FBB pin < 0.9 V, protection circuit active
Over current protection: output current \geq 3.2 A, protection circuit active

3.3) **V\text{\textsubscript{S}}**: Boost Converter

Over voltage protection: V\text{\textsubscript{S}} \geq 18.7 V, protection circuit active
Over current protection: SW pin current \geq 3.5 A, protection circuit active

3.3) **V\text{\textsubscript{AL}}**: Negative Charge Pump

No protection circuits

3.4) **V\text{\textsubscript{GH}}**: Positive Charge Pump

No protection circuits
4. Others

4.1) DLY1 / DLY2 delay time setting
With time delay ($t_{delay}$): DLY1 / DLY2 = open
Without time delay ($t_{delay}$): for each DLY1 / DLY2,

$$C_{delay} = \frac{5.5 \mu A \times t_{delay}}{V_{REF}}$$

Where:
$t_{delay}$ = delay time,
$C_{delay}$ = Capacitor value connected to DLY-pin,
$V_{REF} = 1.213$ V

4.2) $V_{Logic}$ : Buck converter
Output voltage setting:

$$V_{O1} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right)$$

Where:
$V_{REF} = 1.213$ V, $R2 \leq 1.2$ kΩ

Feed-forward capacitance:

$$C_{ff1} = \frac{1}{2 \times \pi \times R1 \times f_{z1}}$$

Where:
$f_{z1}$ = a zero in transfer function

Soft start:
Internal preset
The soft start cycle start after EN1 is asserted and the duration is internally set to 1 ms.

4.3) $V_s$: Boost converter
Output voltage setting:

$$V_{O2} = 1.146 \times \left( 1 + \frac{R3}{R4} \right)$$

Feed-forward capacitance:

$$C_{ff2} = \frac{1}{2 \times \pi \times R3 \times f_{z2}}$$

Where:
$f_{z2}$ = a zero in transfer function

Soft start:
set by external capacitor connected to SS pin
(Soft start active when SS pin voltage < FB voltage)

GD pin:
GD goes L if FB > 1.03 V after delay time DLY2
GD gives Hi-Z if FB ≤ 1.03 V after delay time DLY2
4.4) VGL : Negative Charge Pump
Output voltage setting:
$$VO3 = (-V_{REF}) \times \frac{R5}{R6}, \text{ where } V_{REF} = 1.213 \text{ V}$$

4.5) VGH : Positive Charge Pump
Output voltage setting:
$$VO4 = V_{REF} \times \left( 1 + \frac{R7}{R8} \right), \text{ where } V_{REF} = 1.213 \text{ V}$$

Note: refer to “■ APPLICATION MANUAL” for corresponding resistor.
1. Buck Converter Design

(1) Buck Converter Block Diagram

(2) Inductor Selection

The inductor can range from 10 \( \mu \)H to 15 \( \mu \)H. The current flow through the inductor must below the saturation current rating of the inductor. The maximum current flowing through the inductor can be found from the following formula:

\[
\text{IL}_{\text{MAX}} \geq \frac{\text{IOMAX} \Delta IL}{2}
\]

\[
\Delta IL = \frac{V_{\text{in}} \times V_{\text{out}}}{L} \times \frac{V_{\text{OUT}}}{V_{\text{in}} \times f_{\text{OSC}}}
\]

Where

- \( \text{IL}_{\text{MAX}} \) = Maximum current through inductor [A]
- \( \text{IOMAX} \) = Maximum load current [A]
- \( \Delta IL \) = Inductor ripple current peak-to-peak value [A]
- \( V_{\text{in}} \) = Input voltage [V]
- \( V_{\text{out}} \) = Output voltage [V]
- \( f_{\text{OSC}} \) = switching frequency [Hz] (500 kHz or 750 kHz)
(3) Rectifier Diode Selection

Schottky diode should be used to attain high efficiency. The reverse voltage rating of the diode must be higher than the maximum output voltage of the converter. The required averaged rectified forward current of diode is the product of off-time of Buck converter and the maximum switch current at SWB pin.

\[
\text{Off-time of Buck converter: } D = 1 - \frac{V_{\text{out}}}{V_{\text{in}}} = 1 - D
\]

\[
\text{Maximum output current: } I_{\text{avg}} = (1 - D) \times I_{\text{SWLIM}} = \left(1 - \frac{V_{\text{in}}}{V_{\text{out}}} \right) \times I_{\text{SWLIM}}
\]

A Schottky diode with maximum rectified forward-current of 1.5 A to 2 A should be sufficient for most of applications. The diode forward voltage should be less than 0.7 V in order to prevent damage to IC.

Another requirement for Schottky diode is the power dissipation. The power dissipation can be calculated from the formula below:

\[
P_D = I_{\text{avg}} \times V_F = (1 - D) \times I_{\text{SWLIM}} \times V_F
\]

Where

- \(P_D\) = Power dissipation of the diode [W]
- \(V_F\) = Diode forward voltage [V]
- \(I_{\text{SWLIM}}\) = Minimum over current protection of SWB-pin [A] (2.5 A)

(4) Bootstrap Capacitor Selection

Bootstrap capacitor connected to BOOT pin is charged by integrated synchronous diode with 4 V internal supply. Ceramic capacitor is recommended for less leakage current. The minimum bootstrap capacitor can be calculated by following equation:

\[
C_{\text{BOOT}} \geq \frac{Q_{\text{GATE}} + \frac{I_{\text{DRV (dynamic)}}}{f} + \frac{Q_{\text{DRV (static)}}}{f} + I_{\text{ICBOOH (leak)}}}{V_B - V_f - V_{LS} - V_{\text{min}}}
\]

Where:

- \(C_{\text{BOOT}}\) = bootstrap capacitor value
- \(Q_{\text{GATE}}\) = gate charge of integrated power transistor
- \(f\) = switching frequency (500 kHz or 750 kHz)
- \(I_{\text{DRV (dynamic)}}\) = dynamic current of power transistor driver
- \(Q_{\text{DRV (static)}}\) = static current of power transistor driver
- \(I_{\text{ICBOOH (leak)}}\) = bootstrap capacitor leakage current
- \(V_B\) = internal regulated voltage 4 V
- \(V_f\) = forward voltage drop of bootstrap diode
- \(V_{LS}\) = voltage drop of low-side diode of Buck converter
- \(V_{\text{min}}\) = minimum voltage between BOOT pin and SWB pin

Practically, bootstrap capacitor is selected more than ten times of its minimum value, such that providing sufficient charge for driver and gate of power transistor. With assumption on power used is dominated by charging the gate capacitor of power transistor, the equation can be simplified:

\[
C_{\text{BOOT}} \geq \frac{Q_{\text{GATE}}}{\Delta V}, \text{ where } \Delta V \text{ is the change of boot voltage in switching cycle.}
\]

0.1 μF bootstrap capacitor is recommended for Buck converter in MB39C313. The bootstrap capacitor voltage rating is suggested to be high than input voltage.
(5) Output Capacitor Selection

This IC is designed to work best with ceramic output capacitor. Two 10 μF ceramic output capacitors are recommended for most application. More capacitance can be added so as to reduce voltage drop during load transients.

(6) Output Voltage and Feed Forward Capacitor Selection

- Equivalent circuit of Buck converter error amp block

![Equivalent circuit of Buck converter error amp block](image)

The output voltage of Buck converter can be set by external resistor divider as shown below:

\[ V_{\text{LOGIC}} = V_{\text{REF}} \times \left( 1 + \frac{R_1}{R_2} \right) = 1.213 \times \left( 1 + \frac{R_1}{R_2} \right) \]

R2 is around 1.2 kΩ, and the reference voltage \( V_{\text{REF}} = 1.213 \) V

The lower feedback resistor \( R_2 \) should be around 1.2 kΩ to maintain a minimum load current of 1 mA.  If the loading current is less than 1 mA, the output voltage will rise slightly above the nominal voltage in light load or no load condition.

A feed forward capacitor \( C_{\text{ff}} \) is added parallel to the upper resistor \( R_1 \). The \( C_{\text{ff}} \) sets a zero in the transfer function. This will improve the load transient response and stabilize the converter loop. The value of \( C_{\text{ff}} \) is depending on the inductor and zero frequency \( (f_z) \) required.

For 10 μH inductor, set \( f_z = 8 \) kHz; for 15 μH inductor, set \( f_z = 17 \) kHz.

\[ C_{\text{ff}} = \frac{1}{2 \pi f_z R_1} = \frac{1}{2 \pi \times 8 \text{kHz} \times 1.2 \text{kΩ}} = 9.9 \text{nF} \pm 10 \text{nF} \] (Example of 3.3 V output voltage)

A capacitor value close to the calculated value is chosen.
2. Boost Converter Design

(1) Boost Converter Block Diagram

It is necessary to verify the maximum output current of this converter whether it meets the application requirements. The efficiency of the Boost converter can be read from the graph or employ a worst-case assumption of 80%.

Duty cycle: 
\[ D = 1 - \frac{V_{in} \times \eta}{V_{out}} \]

Maximum output current: 
\[ I_{\text{avg}} = (1 - D) \times \frac{V_{in}}{V_{out}} \times I_{\text{SWLIM}} \]

Peak switch current: 
\[ I_{\text{SWPEAK}} = \frac{V_{in} \times D}{2 \times f_{OSC} \times L} + \frac{I_{out}}{1 - D} \]

Where
- \( D \) = duty cycle
- \( f_{OSC} \) = switching frequency [Hz] (500 kHz or 750 kHz)
- \( L \) = inductor value [H]
- \( \eta \) = estimated Boost converter efficiency (typically 80% minimum)
- \( I_{\text{SWLIM}} \) = minimum switch current limit of SW-pin [A] (= 2.8 A)

The selected components, including the embedded switch, the inductor and external Schottky Diode must be able to handle the peak switching current. The estimation should be based on the minimum input voltage, since the switching current will be the highest in this case.

Limited by the power FET maximum switching current, the maximum output current depends on input voltage and output voltage configuration. Refer to “REFERENCE DATA” section for graphical information. For data reading from reference data, margin is suggested to avoid activating current limit.

Inductor Selection

The inductor can range from 6.8 \( \mu \)H to 22 \( \mu \)H. When selecting the inductor, its saturation current must be higher than the peak switch current \( (I_{\text{SWPEAK}}) \) as shown above. Extra margin is required to cope with high current transients. A more conservative design is to use the maximum SW current limit of 3.5 A as saturation current rating of inductor. Another parameter for choosing inductor is the DC resistance. Usually, lower the DC resistance can result in higher converter efficiency.
(2) Rectifier Diode Selection

Schottky diode should be used to attain high efficiency. The reverse voltage rating of the diode must be higher than the maximum output voltage of the converter. Similar to Buck converter, the required averaged rectified forward current of the Schottky diode is the product of off-time of Boost converter and the maximum switch current at SW pin.

\[
D = 1 - D = \frac{V_{in}}{V_{out}}
\]

Maximum output current: \(I_{avg} = (1 - D) \times I_{SWLIM} \times \frac{V_{in}}{V_{out}} \times I_{SWLIM}\)

A Schottky diode with maximum rectified forward-current of 2A should be sufficient for most applications. Another requirement for Schottky diode is the power dissipation. The power dissipation can be calculated from the formula below:

\[
P_D = I_{avg} \times V_F = (1 - D) \times I_{SWLIM} \times V_F
\]

Where

- \(P_D\) = power dissipation of the diode [W]
- \(V_F\) = diode forward voltage [V]
- \(I_{SWLIM}\) = minimum over current protection of SW-pin [A] (2.8 A)

(3) Output Capacitor Selection

Capacitors with low ESR are recommended. Ceramic capacitor which has low ESR is particularly suitable for this purpose. Typically, three 22 \(\mu\)F ceramic capacitors connected in parallel are placed at the converter output. More capacitance can be added so as to reduce voltage drop during heavy load transients.
(4) Output Voltage and Feed Forward Capacitor Selection

- Equivalent circuit of Boost converter error amp block

![Equivalent circuit of Boost converter error amp block]

The Boost converter output voltage of can be set by external resistor divider as shown below:

\[ V_S = 1.146 \times \left( 1 + \frac{R_3}{R_4} \right) \]

Note: Output overshot due to large input voltage change may be high enough to trigger OVP under certain condition when output setting is close to 18 V.

A feed forward capacitor (Cff2) is added parallel to the upper resistor (R3). The Cff2 sets a zero in the control loop transfer function. This improves the load transient response and stabilizes the converter loop. The value of Cff2 is depending on the inductor and zero frequency (fz2) required.

For 6.8 \( \mu \text{H} \) and 10 \( \mu \text{H} \) inductor, set fz = 10 kHz; for 22 \( \mu \text{H} \) inductor, set fz = 7 kHz.

\[ C_{ff2} = \frac{1}{2 \times \pi \times R_3 \times f_z} = \frac{1}{2 \times \pi \times 680 \text{ k} \Omega \times 10 \text{ kHz}} = 23.4 \text{ pF} \pm 20 \text{ pF} \text{ (Example of 16.5 V output voltage)} \]

A capacitor value close to the calculated value can be used.

(5) Compensation (COMP) Capacitor Selection

The regulator compensation is adjusted by an external component connected to the COMP-pin. This pin is the output of internal trans-conductance error amplifier. By adding a resistor in series will change the internal zero and increases the high-frequency gain. The formula below give the frequency (Fz) at which the resistor increases the high-frequency gain.

\[ F_z = \frac{1}{2 \times \pi \times C_C \times (R_c + 10 \text{ k})} \]

Typically, a 22 nF capacitor is suitable for most applications. If the input voltage is lower, it requires a smaller capacitor value so that it has higher regulator gain.
(6) Soft Start Capacitor Selection

A soft start function is to slow the rate of rising output voltage and minimize the large inrush current at startup. The soft start time is adjustable by connecting external capacitor to SS pin. Soft start capacitor can be estimated by defining the soft start time thought equation below:

\[
C = \frac{I_{SS} \times t_{SS}}{V_{FB}},
\]

Where:
- \(I_{SS}\) = soft start charging current;
- \(t_{SS}\) = soft start time;
- \(V_{FB}\) = voltage at FB pin.

In general, startup time for power supply is larger than 10 us. The startup time of Boost converter of MB39C313 is defined as 1.5 ms.

\[
C = \frac{I_{SS} \times t_{SS}}{V_{FB}} = \frac{15 \mu A \times 1.5 \text{ ms}}{1.146 \text{ V}} = 19.6 \text{ nF}, \text{ therefore, 22 nF soft start capacitor is selected.}
\]

3. Positive Charge Pump Design

(1) Positive Charge Pump Block Diagram

(2) Output Voltage Selection

Theoretically, the maximum output voltage is the sum of input voltage and pumping clock voltage of a charge pump. In MB39C313, the maximum output voltage is \(V_S\) (Boost converter output voltage) + \(V_{SUP} - 2V_{diode}\) which is 17.7 V + 17.7 V + 2(0.4 V) = 34.6 V with typical setting. Due to the regulated voltage control, the output voltage can be configured by equation below:

\[
V_{GH} = V_{REF} \times \left(1 + \frac{R_7}{R_8}\right) = 1.213 \times \left(1 + \frac{R_7}{R_8}\right)
\]

Typically, multiple 2 (x2) function for Positive Charge Pump. Its output voltage will be limited by \(V_S - 2V_{diode} \leq V_{GH} \leq V_S + V_{SUP} - 2V_{diode}\). For other application that requires higher output voltage, MB39C313 allows adding pumping stage by using SW pin. With multiple 3 (x3) function of Positive Charge Pump, the output voltage should be limited by \(2V_S + V_{diode(V_S)} - 2V_{diode} \leq V_{GH} \leq 2V_S + V_{diode(V_S)} + V_{SUP} - 4V_{diode}\).
(3) Pumping Capacitor and Output Capacitor Selection
Ceramic capacitor is recommended for its non-polarized, more stable over temperature, low leakage and small ESR. Choosing a pumping capacitor should consider the required voltage rating and output current loading. For 32 V output voltage setting, the pumping clock voltage is calculated below.

\[ \Delta V_{\text{DRP}} = V_{\text{GH}} - V_{S} + 2(V_{\text{diode}}) = 32 \text{ V} - 17.7 \text{ V} + 2(0.4 \text{ V}) = 15.1 \text{ V} \]

The minimum pumping capacitor is determined by following equation.

\[ C \geq \frac{I_{\text{out}}}{f \times \Delta V_{\text{DRP}}} \]

Where:
- \( I_{\text{out}} \) = the output current
- \( f \) = switching frequency (500 kHz or 750 kHz)
- \( \Delta V_{\text{DRP}} \) = pumping clock voltage

The charge stored on pumping capacitor is transferred to output capacitor cycle-by-cycle. Output capacitor determines output ripple voltage of charge pump. The ripple voltage is estimated by:

\[ V_{\text{ripple}} = \frac{I_{\text{out}}}{2f \times C_{\text{out}}} + I_{\text{out}} \times \text{ESR}_{\text{Cout}} \]

Where:
- \( C_{\text{out}} \) = output filtering capacitance
- \( \text{ESR}_{\text{Cout}} \) = equivalent series resistance of output filtering capacitor

4. Negative Charge Pump Design
(1) Negative Charge Pump Block Diagram

(2) Output Voltage Selection
Recall from functional description, the maximum negative output voltage is \(-V_{\text{DRN}} + V_{\text{diode}}\) ideally, which is \(-12 \text{ V} + 0.4 \text{ V} = -11.6 \text{ V}\). Similar to Positive Charge Pump, the regulated output voltage can be set by equation below:

\[ V_{\text{GL}} = -V_{\text{REF}} \times \frac{R5}{R6} = -1.213 \times \frac{R5}{R6} \]
(3) Pumping Capacitor and Output Capacitor Selection

Selection of pumping capacitor and output capacitor are similar to Positive Charge Pump design.

For −5 V output, $\Delta V_{DRN} = -V_{GL} - V_{diode} = -5 \text{ V} - 0.4 \text{ V} = -5.4 \text{ V}$. The pumping capacitor and output filtering capacitor can be estimated for required application.

Fast input voltage change at power off causes under-shoot (becomes more negative) at Negative Charge Pump output. This under shoot can be reduced by increasing the output capacitance to pumping capacitance ratio. The power off coupling voltage is $V_{IN} - |\Delta V_{DRN}|$. The coupling effect can be estimated as below:

$$\Delta V_{\text{under-shot}} = (V_{IN} - |\Delta V_{DRN}|) \times \frac{C_{\text{pump-cap}}}{C_{\text{pump-cap}} + C_{\text{output-cap}}}$$

Where:
- $\Delta V_{\text{under-shot}}$ = under-shot voltage by power off coupling.
- $\Delta V_{DRN}$ = pumping clock voltage
- $C_{\text{pump-cap}}$ = pumping capacitance
- $C_{\text{output-cap}}$ = output capacitance

In real application, the power off coupling should be negligible due to large loading gate capacitance on panel.

(4) REF Capacitor Selection

REF pin capacitor is used for defining the low frequency gain of reference voltage buffer. 220 nF capacitor is used for stability and performance. Change of capacitance is NOT recommended.

(5) DLY Capacitor Selection

Refer to “Power Up Sequence” section, power up sequence timing is set by capacitor at DLY1 and DLY2 pins. The delay capacitor can be estimated by following equation.

$$C_{\text{delay}} = \frac{5.5 \mu A \times t_{\text{delay}}}{V_{\text{REF}}}$$

Where:
- $t_{\text{delay}}$ = delay time
- $C_{\text{delay}}$ = capacitor connected to DLY-pin
- $V_{\text{REF}} = 1.213 \text{ V}$

(6) Input capacitor Selection

It is recommended to use low ESR capacitor like ceramic capacitor for the input filtering. For AVIN terminal, a 1 μF capacitance connected from AVIN to ground is needed. For the Buck converter, use minimum of two 22 μF ceramic capacitors connected from VINB pin to ground. For the Boost converter, minimum of one 22 μF ceramic capacitor connected from the inductor terminal to ground is recommended.

5. System Design Consideration

(1) Output Glitches when Very Slow Power up Time

A very slow power up time may cause channel output glitches when input voltage across UVLO voltage. Due to slow rise of input voltage at UVLO threshold, the UVLO is easily triggered with switching noise. This undesired UVLO activation will cause glitches at output when channel is loaded.

The main reason is due to the input voltage drop by sudden current draw when channel startup. For maximum output loading, 0.1 Ω equivalent series resistance of power line is able to cause 0.3 V voltage drop. Consider UVLO hysteresis voltage and its response time with margin. For typical setting ($V_{IN} = 12 \text{ V}$, $V_{Logic} = 3.3 \text{ V}$/1.5 A and other channels without load, 0.1 Ω source resistance), it is suggested less than 167 ms input voltage ramp time to avoid such glitches. Refer to “■ TYPICAL APPLICATION CIRCUIT” for typical application setting.
(2) Voltage Overshot at Boost Converter Output during Power Up

A voltage overshot appears at Boost Converter output when input voltage rise time is too fast. This overshot voltage may damage external parts.

Refer to Figure 4, consider the node voltage at power up, both gate voltage of P-type and N-type power FET are zero. With sudden voltage change at input, current flow through inductor and charge up the output capacitor towards input voltage. The P-type power FET will be turned off when output capacitor rise to certain voltage. The charging current continues to flow through the Schottky diode, such that capacitor reaches its peak voltage. As the diode blocks the reverse current, the output capacitor voltage can only be discharged by loading elements.

To avoid this overshot voltage at power up, the rise time of input voltage should be controlled base on RLC resonance frequency of application circuit. No load condition can be used to estimate worst case.

The LC resonance frequency is

\[
\frac{1}{2\pi \sqrt{LC}}
\]

For typical application, \(L = 6.8 \, \mu\text{H}, \, C = 66 \, \mu\text{F}\), the theoretical input rise time should be longer than 133 \(\mu\text{s}\). Margin is suggested for other parasites.

(3) GD FET Isolation

An isolation switch for Boost Converter output is suggested to break current path for application in disable condition. The isolation switch can be controlled by GD pin. Refer to Figure 3 for its application connection.
(4) PCB Layout Recommendation

PCB layout is significant for power supply design. Poor layout would result in generating unwanted voltage and current spikes. This will not only affect DC output voltage, but also radiate EMI to adjacent equipment. Sufficient grounding and minimize parasitic inductance can reduce DC/DC converter switching spike noise.

The following list of rules should be followed when designing power PCB layout

1. Place tracks on the Top Layer and avoid using via or through hole; particularly for nets, such as Input Capacitor (Cin), Inductor (L) and Output Capacitor (Cout).
2. Place the Input Capacitor (Cin) close to the IC, so as to reduce loop current.
3. Place the Schottky diodes close to the SW and SWB respectively, so as to reduce spike noise.
4. Strengthen the ground connection of Input Capacitor (Cin), and Output Capacitor (Cout) with the ground planes. This can be done by placing via holes next to the GND terminals of these components.
5. Place the Schottky Diode and Pumping Capacitor of the two charge pump channels close to IC.
6. The Decoupling Capacitor should be placed near to IC pin of VINB and AVIN. Separate track is required for AVIN and VINB. The GND terminal of AVIN should be placed close to the GND terminal of IC. (Via holes should be placed near to the GND terminals of IC and Capacitors. The connections to internal ground plane should be strengthened at these points.)
7. Feedback paths (i.e. FBB, FB, FBN, FBP) are very sensitive to noise, thus the track should be as short as possible at these terminals. The Output (Vo) feedback line should be placed away from switching components and tracks. Particularly DRN and FBN of the negative charge pump. Use the FREQ pin to separate these two tracks. Similarly, the FBB and SWB can be separated by the EN1 track. Because EN1, EN2 and FREQ are less susceptible to noise.
8. Place wide and short track to connect Boost Converter Output and OS pin.
9. The two ground planes GND and PGND are intersect at the IC thermal pad only.
EXAMPLE OF STANDARD OPERATION CHARACTERISTICS

REFERENCE DATA

(1) Buck Converter Characteristic

**Efficiency vs. Output Current**
VIN = 12 V, V\(_{\text{LOGIC}}\) = 3.3 V, L1 = 10 µH

**Soft Start**
VIN = 12 V, V\(_{\text{LOGIC}}\) = 3.3 V, I\(_{\text{LOAD}}\) = 1.2 A

**PWM Operation**
Continuous Mode
VIN = 12 V, V\(_{\text{LOGIC}}\) = 3.3 V, I\(_{\text{LOAD}}\) = 1.5 A

Discontinuous Mode
VIN = 12 V, V\(_{\text{LOGIC}}\) = 3.3 V, I\(_{\text{LOAD}}\) = 45 mA

**Output Voltage vs. Output Current**
VIN = 8 V
VIN = 10 V
VIN = 12 V
VIN = 14 V

Load Current Io (A) vs. Output Voltage Vo (V)
(2) Boost Converter Characteristic

Efficiency vs. Output Current
VIN = 12 V, V_S = 17.7 V, L2 = 6.8 μH

Soft Start
VIN = 12 V, V_S = 17.7 V, I_LOAD = 1.2 A, C_SS = 22 nF

PWM Operation
Continuous Mode
VIN = 12 V, V_S = 17.7 V, I_LOAD = 1.5 A

PWM Operation
Discontinuous Mode
VIN = 12 V, V_S = 17.7 V, I_LOAD = 10 mA

Output Voltage vs. Output Current

Note: Output current is limited in low input voltage configuration. Refer to “APPLICATION MANUAL” for Boost converter design.
(3) Negative Charge Pump Characteristic

Output Voltage vs. Output Current

$V_{GL} = -5\text{ V}$

Output Ripple Voltage

$V_{IN} = 12\text{ V}, V_{GL} = -5\text{ V}, I_{LOAD} = 50\text{ mA}$

(4) Positive Charge Pump Characteristic

Output Voltage vs. Output Current

$V_{SUP} = 17.7\text{ V}, V_{GH} = 32\text{ V}, I_{LOAD} = 50\text{ mA}$

Output Ripple Voltage

$V_{IN} = 12\text{ V}, V_{SUP} = 17.7\text{ V}, V_{GH} = 32\text{ V}, I_{LOAD} = 50\text{ mA}$
(5) Converter Load Transient Characteristic

**Buck Converter**
Load Transient Response

VIN = 12 V, V\_LOGIC = 3.3 V, Co = 2 \times 10 \, \mu F,
L1 = 10 \, \mu H, FREQ = High

**Boost Converter**
Load Transient Response

VIN = 12 V, V\_S = 17.7 V, Co = 3 \times 22 \, \mu F,
L2 = 6.8 \, \mu H, C\_comp = 22 \, nF, FREQ = High

**Negative Charge Pump**
Load Transient Response

VIN = 12 V, V\_L = -5 V, FREQ = High

**Positive Charge Pump**
Load Transient Response

VIN = 12 V, V\_SUP = 17.7 V,
V\_GH = 32 V, FREQ = High
(6) Converter Line Transient Characteristic

Buck Converter
Line Transient Response

\[ V_{\text{LOGIC}} = 3.3 \text{ V}, \quad I_{\text{LOAD}} = 1.5 \text{ A}, \quad C = 2 \times 10 \mu\text{F}, \quad L_1 = 10 \mu\text{H}, \quad \text{FREQ} = \text{High} \]

Boost Converter
Line Transient Response

\[ V_S = 17.7 \text{ V}, \quad I_{\text{LOAD}} = 1.5 \text{ A}, \quad C = 3 \times 22 \mu\text{F}, \quad L_2 = 6.8 \mu\text{H}, \quad C_{\text{comp}} = 22 \text{nF}, \quad \text{FREQ} = \text{High} \]

Negative Charge Pump
Line Transient Response

\[ V_{\text{GL}} = -5 \text{ V}, \quad I_{\text{LOAD}} = 50 \text{ mA}, \quad \text{FREQ} = \text{High} \]

Positive Charge Pump
Line Transient Response

\[ V_{\text{SUP}} = 17.7 \text{ V}, \quad V_{\text{GHI}} = 32 \text{ V}, \quad I_{\text{LOAD}} = 50 \text{ mA}, \quad \text{FREQ} = \text{High} \]
(7) Power-up Sequence

Power-up Sequence
VIN = EN1 = EN2 = 12 V
All channel without load

Power-up Sequence
EN2 Enabled Separately
All channel without load

Power-up Sequence
VIN = EN1 = EN2 = 12 V
ILoad(VLogic) = 1.5 A, ILoad(VS) = 1.5 A
ILoad(VGL) = 50 mA, ILoad(VGH) = 50 mA

Power-up Sequence
EN2 Enabled Separately
ILoad(VLogic) = 1.5 A, ILoad(VS) = 1.5 A
ILoad(VGL) = 50 mA, ILoad(VGH) = 50 mA
**TYPICAL APPLICATION CIRCUIT**

![TYPICAL APPLICATION CIRCUIT Diagram](image-url)
### Part List

<table>
<thead>
<tr>
<th>Count</th>
<th>Designator</th>
<th>Item Specification</th>
<th>Part Value</th>
<th>Package</th>
<th>Part number</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>U1</td>
<td>IC, Bias Power Supply for LCD</td>
<td>MB39C313</td>
<td>TSSOP28P</td>
<td>MB39C313</td>
<td>FML</td>
</tr>
<tr>
<td>2</td>
<td>C1, C24</td>
<td>Capacitor, Ceramic, 50 V, X5R, 10%</td>
<td>1 μF</td>
<td>1206</td>
<td>C3216X5R1H105K</td>
<td>TDK</td>
</tr>
<tr>
<td>2</td>
<td>C10, C11</td>
<td>Capacitor, Ceramic, 10 V, B, 20%</td>
<td>10 μF</td>
<td>0805</td>
<td>C2012JB1A106K</td>
<td>TDK</td>
</tr>
<tr>
<td>6</td>
<td>C7, C8, C13, C14, C15, C16</td>
<td>Capacitor, Ceramic, 25V, B, 20%</td>
<td>22 μF</td>
<td>1210</td>
<td>C3225JB1E226M</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>C17</td>
<td>Capacitor, Ceramic, 50 V, CH, 5%</td>
<td>22 pF</td>
<td>0603</td>
<td>C1608CH1H220J</td>
<td>TDK</td>
</tr>
<tr>
<td>8</td>
<td>C18, C22, C23, C25, C26, C27, C28, C29</td>
<td>Capacitor, Ceramic, 50 V, B, 10%</td>
<td>0.47 μF</td>
<td>1206</td>
<td>C3216JB1H474K</td>
<td>TDK</td>
</tr>
<tr>
<td>2</td>
<td>C2, C3</td>
<td>Capacitor, Ceramic, 50 V, B, 10%</td>
<td>22 nF</td>
<td>0603</td>
<td>C1608JB1H223K</td>
<td>TDK</td>
</tr>
<tr>
<td>3</td>
<td>C4, C5, C12</td>
<td>Capacitor, Ceramic, 50 V, B, 10%</td>
<td>10 nF</td>
<td>0603</td>
<td>C1608JB1H103K</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>C6</td>
<td>Capacitor, Ceramic, 25 V, B, 10%</td>
<td>220 nF</td>
<td>0603</td>
<td>C1608JB1E224K</td>
<td>TDK</td>
</tr>
<tr>
<td>1</td>
<td>C9</td>
<td>Capacitor, Ceramic, 50 V, B, 10%</td>
<td>0.1 μF</td>
<td>0603</td>
<td>C1608JB1H104K</td>
<td>TDK</td>
</tr>
<tr>
<td>2</td>
<td>D1, D2</td>
<td>Diode, Schottky Rectifier, 3 A, 30 V</td>
<td>MBRA340T3</td>
<td>SMA-403D</td>
<td>MBRA340T3</td>
<td>On-Semi</td>
</tr>
<tr>
<td>3</td>
<td>D3, D4, D5</td>
<td>Diode, Dual Schottky, 200 mA, 30 V</td>
<td>BAT54S</td>
<td>SOT23</td>
<td>BAT54S</td>
<td>On-Semi</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>Inductor, SMT, 6.5 A, 35 mΩ</td>
<td>10 μH</td>
<td>10x10.2</td>
<td>CDRH104R-100NC</td>
<td>Sumida</td>
</tr>
<tr>
<td>1</td>
<td>L2</td>
<td>Inductor, SMT, 4.4 A, 40 mΩ</td>
<td>6.8 μH</td>
<td>7.5x8</td>
<td>PLC-0745-6R8S</td>
<td>NEC</td>
</tr>
<tr>
<td>6</td>
<td>R2, R12, R14, R17, R21, R23</td>
<td>Resistor, 1 A, Chip, 0.5%</td>
<td>0R</td>
<td>0603</td>
<td>RK73Z1J</td>
<td>KOA</td>
</tr>
<tr>
<td>1</td>
<td>R8</td>
<td>Resistor, 2 A, Chip, 0.5%</td>
<td>0R</td>
<td>0805</td>
<td>RK73Z2J</td>
<td>KOA</td>
</tr>
<tr>
<td>1</td>
<td>R10</td>
<td>Resistor, Chip, 1/16 W, 0.5%</td>
<td>56 K</td>
<td>0603</td>
<td>RR0816P-563-D</td>
<td>SSM</td>
</tr>
<tr>
<td>1</td>
<td>R11</td>
<td>Resistor, Chip, 1/10 W, 0.5%</td>
<td>680 K</td>
<td>0603</td>
<td>RK73G1JTTD6803D</td>
<td>KOA</td>
</tr>
<tr>
<td>2</td>
<td>R13, R27</td>
<td>Resistor, Chip, 1/16 W, 0.5%</td>
<td>51 K</td>
<td>0603</td>
<td>RR0816P-513-D</td>
<td>SSM</td>
</tr>
<tr>
<td>1</td>
<td>R19</td>
<td>Resistor, Chip, 1/10 W, 0.5%</td>
<td>620 K</td>
<td>0603</td>
<td>RK73G1JTTD6203D</td>
<td>KOA</td>
</tr>
<tr>
<td>1</td>
<td>R20</td>
<td>Resistor, Chip, 1/16 W, 0.5%</td>
<td>150 K</td>
<td>0603</td>
<td>RR0816P-154-D</td>
<td>SSM</td>
</tr>
<tr>
<td>1</td>
<td>R26</td>
<td>Resistor, Chip, 1/10 W, 0.5%</td>
<td>1 M</td>
<td>0603</td>
<td>RK73G1JTTD1004D</td>
<td>KOA</td>
</tr>
<tr>
<td>2</td>
<td>R28, R29</td>
<td>Resistor, Chip, 1/16 W, 0.5%</td>
<td>100 K</td>
<td>0603</td>
<td>RR0816P-104-D</td>
<td>SSM</td>
</tr>
<tr>
<td>1</td>
<td>R5</td>
<td>Resistor, Chip, 1/16W, 0.5%</td>
<td>2 K</td>
<td>0603</td>
<td>RR0816P-202-D</td>
<td>SSM</td>
</tr>
<tr>
<td>1</td>
<td>R6</td>
<td>Resistor, Chip, 1/16W, 0.5%</td>
<td>1.1 K</td>
<td>0603</td>
<td>RR0816P-112-D</td>
<td>SSM</td>
</tr>
</tbody>
</table>
### (Continued)

<table>
<thead>
<tr>
<th>Count</th>
<th>Designator</th>
<th>Item Specification</th>
<th>Part Value</th>
<th>Package</th>
<th>Part number</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R7</td>
<td>Resistor, Chip, 1/16W, 0.5%</td>
<td>62R</td>
<td>0603</td>
<td>RR0816Q-620-D</td>
<td>SSM</td>
</tr>
<tr>
<td>2</td>
<td>J1, J2</td>
<td>Jumper</td>
<td>—</td>
<td>HDR1X2</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>2</td>
<td>J3, J4</td>
<td>Jumper</td>
<td>—</td>
<td>HDR1X3</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>C19</td>
<td>—</td>
<td>220 nF</td>
<td>0603</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>C20</td>
<td>—</td>
<td>1 μF</td>
<td>1206</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>C21</td>
<td>—</td>
<td>22 μF/25 V</td>
<td>1210</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>Q1</td>
<td>P-ch MOSFET</td>
<td>SI2343DS</td>
<td>SOT23</td>
<td>Si2343DS</td>
<td>Vishay</td>
</tr>
<tr>
<td>No Mount</td>
<td>R15</td>
<td>—</td>
<td>100 K</td>
<td>0603</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>R16</td>
<td>—</td>
<td>1 M</td>
<td>0603</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>R22</td>
<td>—</td>
<td>0R</td>
<td>0603</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>No Mount</td>
<td>R24</td>
<td>—</td>
<td>0R</td>
<td>0603</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

FML : FUJITSU MICROELECTRONICS LIMITED  
TDK : TDK Corporation  
OnSemi : ON Semiconductor Corporation  
Sumida : Sumida Corporation  
NEC : NEC Electronics Corporation  
KOA : KOA Corporation  
SSM : SUSUMU Co. Ltd.  
Vishay : Vishay Intertechnology, Inc.
**LAND PATTERN**

The MB39C313 has an exposed thermal pad zone on the bottom side of the IC. This area has to be soldered onto the PCB board to enhance heat dissipation. The via should be placed in the thermal pad. These via assist heat dissipation towards the bottom layer of the PCB. Via and copper pad size may be adjusted according to PCB constraints.

- Land pattern design example
■ USAGE PRECAUTIONS

1. Never use setting exceeding maximum rated conditions.
   Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Use the devices within recommended conditions
   It is recommended that devices be operated within recommended conditions. Exceeding the recommended operating condition may adversely affect devices reliability. Nominal electrical characteristics are warranted within the range of recommended operating conditions otherwise specified on each parameter in the section of electrical characteristics.

3. Design the ground line on printed circuit boards with consideration of common impedance.

4. Take appropriate static electricity measures.
   Containers for semiconductor materials should have anti-static protection or be made of conductive material. After mounting, printed circuit boards should be stored and shipped in conductive bags or containers. Work platforms, tools, and instruments should be properly grounded. Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not apply negative voltages
   The use of negative voltages below -0.3 V may activate parasitic transistors on the device, which can cause abnormal operation.

■ ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part number</th>
<th>Package</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB39C313PFTH</td>
<td>28-pin plastic TSSOP</td>
<td>Exposed PAD</td>
</tr>
</tbody>
</table>

■ EV BOARD ORDERING INFORMATION

<table>
<thead>
<tr>
<th>EV Board Part No.</th>
<th>EV Board version No.</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>MB39C313EVB-01</td>
<td>MB39C313EVB-01 Rev.1.2</td>
<td>TSSOP-28</td>
</tr>
</tbody>
</table>

■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

The LSI products of FUJITSU MICROELECTRONICS with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenylethers (PBDE).

A product whose part number has trailing characters “E1” is RoHS compliant.
MARKING FORMAT (LEAD FREE VERSION)

INDEX Lead-free version

MB39C313

E1

XXXX XXX
The part number of a lead-free product has the trailing characters “E1”.

“ASSEMBLED IN CHINA” is printed on the label of a product assembled in China.
■ MB39C313PFTH RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

[FUJITSU MICROELECTRONICS Recommended Mounting Conditions]

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mounting Method</td>
<td>IR (infrared reflow), warm air reflow</td>
</tr>
<tr>
<td>Mounting times</td>
<td>2 times</td>
</tr>
<tr>
<td>Storage period</td>
<td>Before opening: Please use it within two years after manufacture.</td>
</tr>
<tr>
<td></td>
<td>From opening to the 2nd reflow: Less than 8 days</td>
</tr>
<tr>
<td></td>
<td>When the storage period after opening was exceeded: Please process within 8 days after baking (125 °C ± 3 °C, 24hrs + 2H/-0H)</td>
</tr>
<tr>
<td></td>
<td>Baking can be performed up to two times.</td>
</tr>
<tr>
<td>Storage conditions</td>
<td>5 °C to 30 °C, 70%RH or less (the lowest possible humidity)</td>
</tr>
</tbody>
</table>

[Parameters for Each Mounting Method]

IR (infrared reflow)

![Graph showing temperature profiles for IR reflow]

H rank : 260 °C Max

(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60s to 180s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10s or less
(d') : Temperature 230 °C or more, 40s or less or Temperature 225 °C or more, 60s or less or Temperature 220 °C or more, 80s or less
(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

Manual soldering (partial heating method)

<table>
<thead>
<tr>
<th>Item</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage period</td>
<td>Before opening: Within two years after manufacture.</td>
</tr>
<tr>
<td></td>
<td>Between opening and mounting: Within two years after manufacture. (No need to control moisture during the storage period because of the partial heating method.)</td>
</tr>
<tr>
<td>Storage conditions</td>
<td>5 °C to 30 °C, 70%RH or less (the lowest possible humidity)</td>
</tr>
<tr>
<td>Mounting conditions</td>
<td>Temperature at the tip of a soldering iron: 400 °C max Time: Five seconds or below per pin*</td>
</tr>
</tbody>
</table>

*: Make sure that the tip of a soldering iron does not come in contact with the package body.
### PACKAGE DIMENSIONS

28-pin plastic TSSOP

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead pitch</td>
<td>0.65 mm</td>
</tr>
<tr>
<td>Package width × package length</td>
<td>4.40 mm × 9.70 mm</td>
</tr>
<tr>
<td>Lead shape</td>
<td>Gullwing</td>
</tr>
<tr>
<td>Sealing method</td>
<td>Plastic mold</td>
</tr>
<tr>
<td>Mounting height</td>
<td>1.20 mm Max</td>
</tr>
<tr>
<td>Weight</td>
<td>0.12 g</td>
</tr>
</tbody>
</table>

![Image of 28-pin plastic TSSOP](FPT-28P-M20)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) *: These dimensions do not include resin protrusion.

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
# CONTENTS

- DESCRIPTION .................................................................................................................................................. 1
- FEATURES ...................................................................................................................................................... 1
- APPLICATIONS .................................................................................................................................................. 1
- PIN ASSIGNMENT ......................................................................................................................................... 2
- PIN DESCRIPTIONS ....................................................................................................................................... 3
- I/O PIN EQUIVALENT CIRCUIT DIAGRAM ................................................................................................. 4
- BLOCK DIAGRAM .......................................................................................................................................... 7
- FUNCTIONAL DESCRIPTIONS ...................................................................................................................... 8
- ABSOLUTE MAXIMUM RATINGS .................................................................................................................. 11
- RECOMMENDED OPERATION CONDITIONS ............................................................................................. 12
- ELECTRICAL CHARACTERISTICS ............................................................................................................... 13
- TYPICAL CHARACTERISTICS .................................................................................................................... 17
- SET UP ......................................................................................................................................................... 19
- APPLICATION MANUAL .................................................................................................................................. 22
- EXAMPLE OF STANDARD OPERATION CHARACTERISTICS ........................................................................ 33
- TYPICAL APPLICATION CIRCUIT ................................................................................................................ 39
- LAND PATTERN .............................................................................................................................................. 42
- USAGE PRECAUTIONS ..................................................................................................................................... 43
- ORDERING INFORMATION .......................................................................................................................... 43
- EV BOARD ORDERING INFORMATION ...................................................................................................... 43
- RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION ............................................................ 43
- MARKING FORMAT (LEAD FREE VERSION) ................................................................................................ 44
- LABELING SAMPLE (LEAD FREE VERSION) .................................................................................................. 45
- MB39C313PFTH RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL .................. 46
- PACKAGE DIMENSIONS ............................................................................................................................... 47