

FLEXRAY
32-BIT MICROCONTROLLER
FLEXRAY-FPGA-EVA-KIT-369

**INTERRUPT USAGE ON
FLEXRAY CC**

APPLICATION NOTE

Revision History

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1 Introduction

The FlexRay™ Communication Controller (CC) supports Interrupt processing for various states. This Application Notes describes the initialisation and usage of FlexRay CC interrupts at the Fujitsu Evaluation board “FLEXRAY-FPGA-EVA-KIT-369”.

The software example “Gateway-dyn-int” is showing the receive interrupt usage for dynamic message buffers.

2 ERAY Interrupts

This chapter describes the interrupt usage.

2.1 Hardware

The FLEXRAY-FPGA-EVA-KIT-369 follows a modular concept. The MCU board hooks the MB91F369GA host MCU; the FPGA main board hooks the FPGA based FlexRay CC. The access from host MCU to the FlexRay CC is done via 32-bit data bus interface. The two CC Interrupt lines (Called INTA and INTB at FPGA main board) are connected to external Interrupts at MB91F369GA series (INT2 and INT3).

The Interrupt pins are also routed to the connector J55 at FPGA Main board.

Pin 29: Interrupt A

Pin 31: Interrupt B

E-Ray	FPGA CC	MB91F369GA
Interrupt Line 0	Interrupt A / J55.P29	Int2 / pin 70
Interrupt Line 1	Interrupt B / J55.P31	Int3 / pin 71

Table 2-1: Interrupt connection MB91F369GA / FPGA Communication Controller

2.1.1 Hardware modification

To ensure a proper Level detection a MCU pins, follow the instructions in application note mcu-an-300010-e-vxx-flexray-int-modify.

2.2 Software

Using the FlexRay Communication Controller (CC) interrupt, the interrupt resources have to be initialised. Not only at FlexRay CC side, but also the external Interrupt at MB91F369GA host MCU.

2.2.1 FlexRay CC interrupt

The interrupt concept of the CC includes a user selection which interrupt resource is connected to which interrupt line. Two timers are available to issue interrupts by certain (periodic) intervals. Via the Stop Watch Function, an interrupt can be processed via external signal.

Note:

The Stop Watch function is currently not available at a FPGA pin!

2.2.1.1 FlexRay CC Interrupt Register

There are 12 Interrupt registers available:

- EIR (Error Interrupt Register)
- SIR (Status Interrupt Register)
- EILS (Error Interrupt Line Select)
- SILS (Status Interrupt Line Select)
- EIES (Error Interrupt Enable Set)
- EIER (Error Interrupt Enable Reset)
- SIES (Status Interrupt Enable Set)
- SIER (Status Interrupt Enable Reset)
- ILE (Interrupt Line Enable)
- T0C (Timer 0 Configuration)
- T1C (Timer 1 Configuration)
- STPW (Stop Watch Register)

There are two different categories of interrupt sources; error interrupt and status interrupts.

The EIR and the SIR Register contain the interrupt flags. They indicate an interrupt request. In case of an interrupt request the flag is set to H-Level. The flag must be cleared by writing '1' to the bit position.

To enable / disable the various interrupt sources, there are two register. To enable the interrupt sources use the EIES / SIES register. Disabling is done via EIER / SIER Register.

Note:

Enable / disable of FlexRay CC interrupts is done in different register!

Via the Interrupt line select register (EILR, SILR), interrupt sources can be assigned to the interrupt lines. By default, status interrupts are assigned to interrupt line 0, error interrupts are assigned to interrupt line 1.

The two interrupt lines (line 0 and line 1) are enabled / disabled via the ILE register

The timer interrupts are configured via the T0C and T1C register. Base of these timers are MT (Macrotick).

The setup of the interrupts can be done via initialisation phase (CONFIG STATE) or during run phase (e.g. READY STATE).

Receive, transmit and MBSI Interrupts must be set for each message buffer, individually. Via the MBI (Message Buffer Interrupt in WHRS1 register) bit, it is possible to activate the interrupt for the dedicated message buffer.

2.2.1.2 Setup of interrupts

Following example illustrates the steps to initialise and use the interrupts.

Setup a receive interrupt:

1. The RXI interrupt is a status interrupt.
2. Check RXI flag in SIR register if a pending interrupt request is set / clear interrupt request
3. Select interrupt line for RXI interrupt in Register SILS (RXIL bit). By default status interrupts are set to interrupt line 1.
4. Enable RXI interrupt in SIES register (RXIE bit). Be aware to disable this RXI interrupt the SIER register must be used!
5. Enable Interrupt Line via ILE bit.
6. The receive enable interrupt is now setup. All message buffers with enabled MBI bit in WRHS1 register (header section) will issue a receive interrupt.

Note:

RX, TX and MBSI Interrupts will issue an interrupt request in case the MBI bit of the message buffer is set to 1 (WRHS1 register)

2.2.2 Host MCU interrupt

At host MCU (MB91F369GA) the external Interrupt channel 2 must be set up when activating Interrupt line A of FlexRay CC. External Interrupt channel 3 for FlexRay CC Interrupt B. The FlexRay CC Interrupt signal is active high.

2.2.2.1 External Interrupt Register

The External interrupt function in MB91F369GA series consist of three register.

- Enable Interrupt Request Register (EINR)
- External Interrupt Request Register (EIRR)
- External Level Register (ELVR)

Enabling of the external interrupt is done via EINR register.

A pending interrupt request is shown in EIRR register. Via the ELVR register the external signal detection is set (High-, Low-Level, rising-, falling edge)

Note:

In MB91F369GA series the Port Function Register (PFRx) defines whether to use I/O port or resource functionality.

2.2.2.2 Setup of external Interrupts

To initialise the external Interrupt following steps must proceed:

1. Set External level detection in ELVR register (High-, Low-Level, rising-, falling edge)
2. Set Port function to external Interrupt in PFRK register
3. Clear request flag in EIRR register
4. Enable external interrupt via ENIR register

In addition to this initialisation the interrupt level of the external interrupt must be defined in the corresponding ICR (Interrupt Control Register) register. Also an interrupt service routine (ISR) must be implemented.

Note:

The interrupt request flag of the external interrupt (EIRR register) must be clear by application inside the ISR. Furthermore the ERAY CC interrupt request flag must be cleared!

2.2.3 Software flow

To use the ERAY CC interrupts the interrupts of the FlexRay CC must be set up accordingly. Furthermore the external Interrupt of MB91F369GA must be set up. (Including interrupt level and interrupt service routine)

In case of an interrupt request, the ISR of the external interrupt is executed. After executing the interrupt request flag of the FlexRay CC *and* MB91F369GA external interrupt flag must be cleared in the ISR, before leaving the ISR. Otherwise a further interrupt request will be issued directly after leaving this ISR.

3 Appendix

3.1 Documentation

For more information refer to following manuals:

- MB91360 Series Hardware Manual
- ERAY Users Manual
- User guide of FLEXRAY-FPGA-EVA-KIT-369

3.2 Abbreviations

FME	Fujitsu Microelectronics Europe GmbH
MCU	Microcontroller Unit
ASSP	Application Specific Standard Product
FPGA	Field Programmable Gate Array
PCB	Printed Circuit Board
CC	Communication Controller
E-Ray	FlexRay Communication Controller provided by company BOSCH
HOST	part of an ECU where the application software is executed
FlexRay	automotive network

3.3 Tables

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