

SD Multi-standard Decoder LSI

Specification:

System CPU Platform

ARM926EJ-S, 324 ~ 405MHz
(maximum achievable in 90nm)
Java acceleration
DDR/SDR 128MB

Dual Video Decoder

H.264 Base& Main, D1 @30fps
VC1 AP, D1 @30fps
MPEG-4 ASP, D1 @30fps
MPEG-2, MP, D1 @30fps
JPEG

Video Encoder

HW/SW Based QVGA H.263 Codec

Audio Codec

MP1/2/3,
AAC,
AMR,
others

Display Control

TV In / Camera In
TV Out / LCD out
Resize
2D/OSD
PIP

System Decoder

TS Demux (CSA) x 2

Others

Storage: NAND, SD/MMC, HDD
IO: I2C, UART, GPIO, etc
USB2.0 Host/Slave+PHY
SDIO
Ethernet

System Functions

JTAG

PLL & Power Management

TIMER

Watch Dog

RTC

NOR/SRAM/
ATA/PCMCIA

DDR/SDR
SDRAM

Connectivity Function

USB2.0 HS

Ethernet

System CPU Platform

ARM926EJ-S	I/D-Cache 16kBx2	MMU
	I/D-TCM 8kBx2	

DMA 8ch	On-chip SRAM	Bus Control	Memory Control
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Video Multi-Standard Decoder

Hardware Decoding Pipeline

RISC
CPU

RISC
CPU

Display / TV Output Control

2D/OSD

Resizer

NTSC/PAL
Encoder

LCD output

Camera / TV Input Control

656 Input

Camera Input

TS Demux

DVB DES (CSA)

Audio IO

I2S_i I2S_o

Storage Function

MMC/SD/SDIO

NAND

Security

SMART Card

DRM

System IO Functions

PWM

GPIO

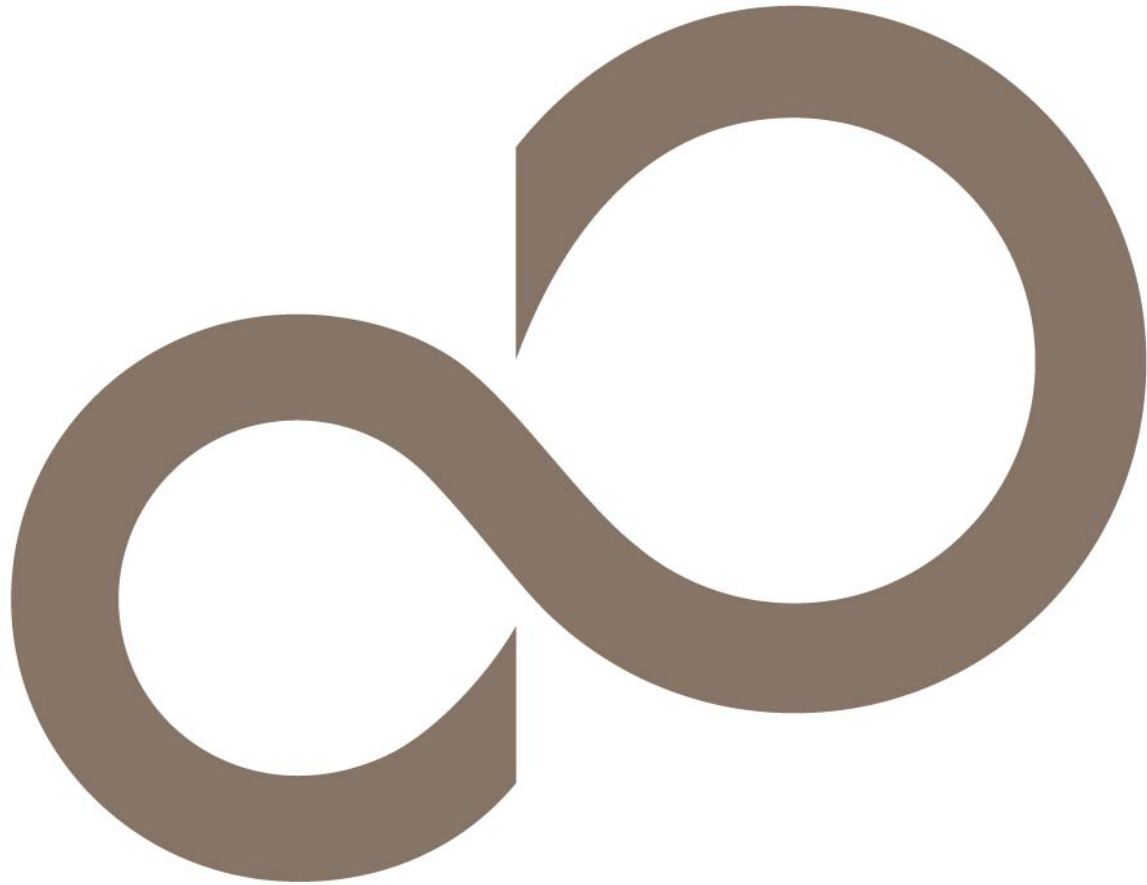
Keypad

UART

UART

I2C

SPI



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