32M-bit/64M-bit Mobile FCRAM™ Adopting a Multiplexed Address and Data Bus

MB82DBS02154E/MB82DBS04154E

Burst mode Mobile FCRAMs adopting multiplexed address and data bus to save pin count

Introduction

Mobile FCRAM is a pseudo SRAM featuring low power consumption for mobile phone applications. FUJITSU first introduced Mobile FCRAM products in 2000. The Mobile FCRAM has SRAM interface that is compatible with NOR-type Flash memory. MCP (Multi-Chip Package) products consisting of Mobile FCRAM and Flash memory have been highly successful in the mobile phone market.

Fig.1 presents an example of a mobile phone block diagram.

Mobile FCRAM products are available from 16M-bit to 256M-bit and have been utilized in various applications. Mobile FCRAM featuring high-speed data transfer in burst mode and low power consumption is the optimal memory not only for today's mobile phones, but also for portable digital media applications operated by batteries.

Figure 1 Mobile Phone Block Diagram (Example)

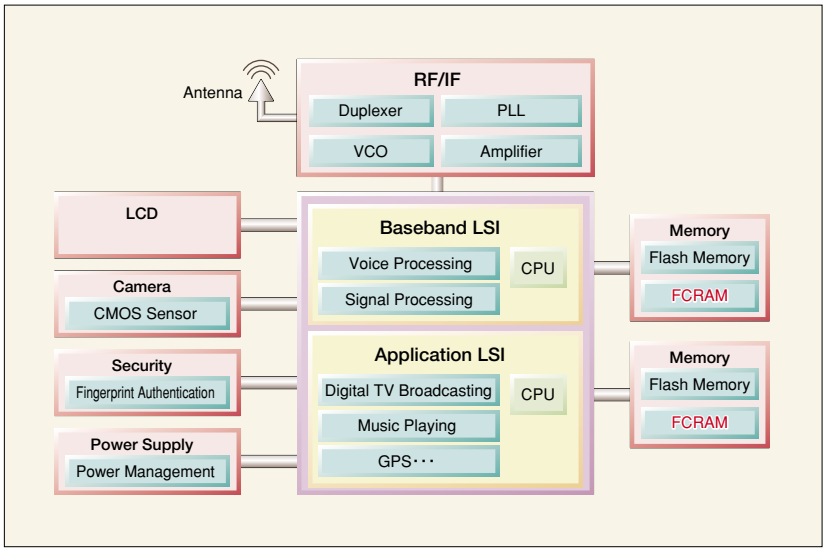
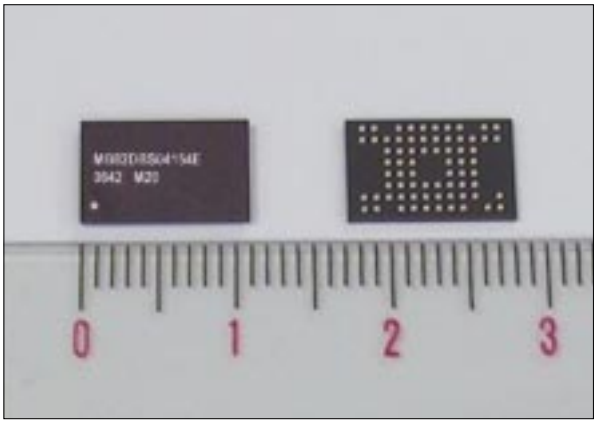


Photo 1 MB82DBS04154E Package View



New 32M-bit/64M-bit Mobile FCRAM Products

We have added new 32M-bit and 64M-bit Mobile FCRAM products to our product line. The MB82DBS02154E and MB82DBS04154E are within the current major pseudo SRAM density range and satisfy the need for medium range that low-density SRAM and large-density SDRAM don't support.

Both products have 1.8V operation and adopt a 16-bit multiplexed address and data bus for I/O bus configuration. A synchronous burst mode function is adopted in addition to asynchronous mode.

These products conform to COSMORAM (Common Specifications for Mobile RAM) Revision 3, the common interface specifications for pseudo SRAM adopting burst mode. Products conforming to COSMORAM are compatible with each other even if the suppliers are different. Since suppliers use common specifications, they can act as alternative sources for each other, helping ensure a stable market supply.

In addition, customers can use common design boards, improving the design efficiency.

Multiplexed Address and Data Bus

The multiplexed address and data bus is the bus configuration that address pins are shared with DQ signals. By using the shared pins, total pin count is reduced compared to conventional products that use a separate address and data bus configuration.

Table 1 presents a comparison of pin count between multiplexed A/DQ and separate A/DQ products. Multiplexed address and data bus products have a smaller pin count compared to the same density products with a separate address and data bus configuration.

The multiplexed address and data bus products reduce the workload of complicated routing design for board or SiP (System in Package) design. Since a multiplexed address and data bus configuration also saves the routing space

Table 1 Comparison of Pin Count between Multiplexed A/DQ and Separate A/DQ

	FUJITSU Mobile FCRAM MB82DBS04154E	Competitor's Low Power SDRAM	FUJITSU Mobile FCRAM MB82DBS04164E
Density	64M-bit (4M×16)	64M-bit (4M×16)	64M-bit (4M×16)
A/DQ Bus Configuration	Multiplexed A/DQ	Separate A/DQ	Separate A/DQ
Count of signal pins	31 pins	38 pins	47 pins

*Count of signal pins indicates the total of address pins, DQ pins, and control pins (excluding power supply, NC, and DU).

Figure 2 Pin Assignment of Multiplexed Address and Data Bus (MB82DBS04154E)

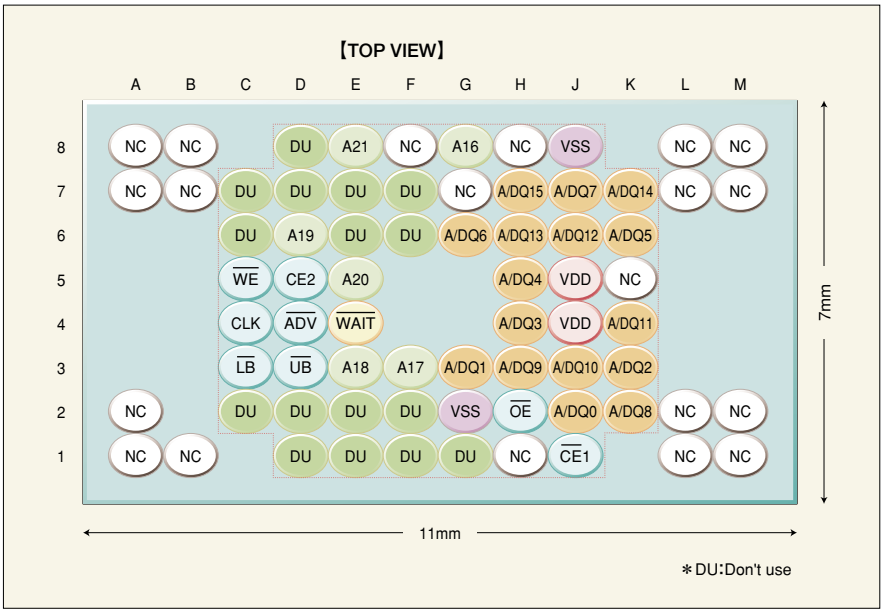
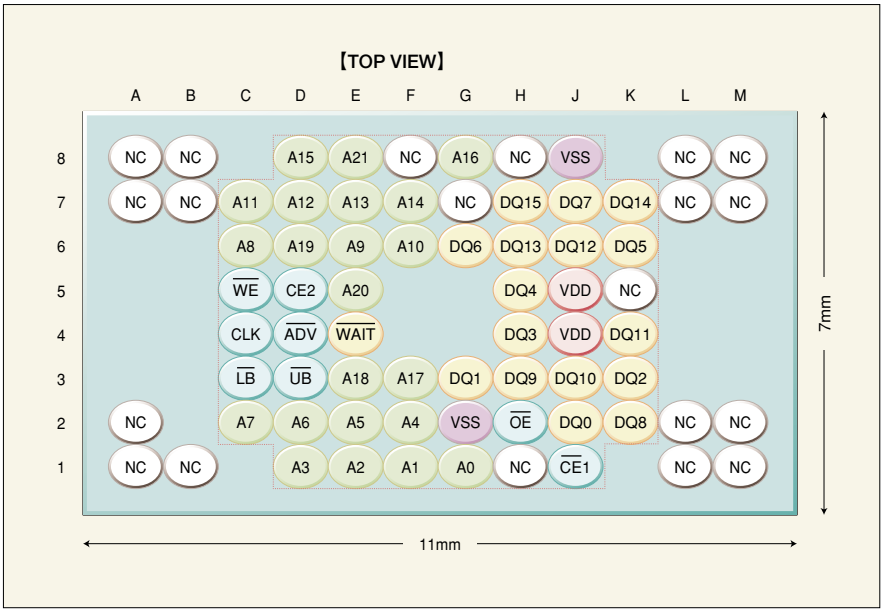


Figure 3 Pin Assignment of Separate Address and Data Bus (MB82DBS04164E)



on the board, it will help reduce development cost. The signals must be controlled so as to avoid bus conflict in the read operation, since the same pins are used for address input and data input/output.

Figs.2 and **3** present the pin assignments of the FBGA package products for a multiplexed address and data bus (MB82DBS04154E) and separate address and data bus (MB82DBS04164E).

Fig.4 presents the read timing of the MB82DBS04154E. To avoid bus conflict between the address input signals and data output signals on the A/DQ pins, the control signals must be controlled. For comparison, **Fig. 5** presents the timing for the MB82DBS04164E.

Products Features

- Conforms to COSMORAM Rev. 3
- SRAM interface (synchronous mode/asynchronous mode)
- Organization:
  2M words×16-bit (MB82DBS02154E)
  4M words×16-bit (MB82DBS04154E)

Figure 4 Read Timing for MB82DBS04154E

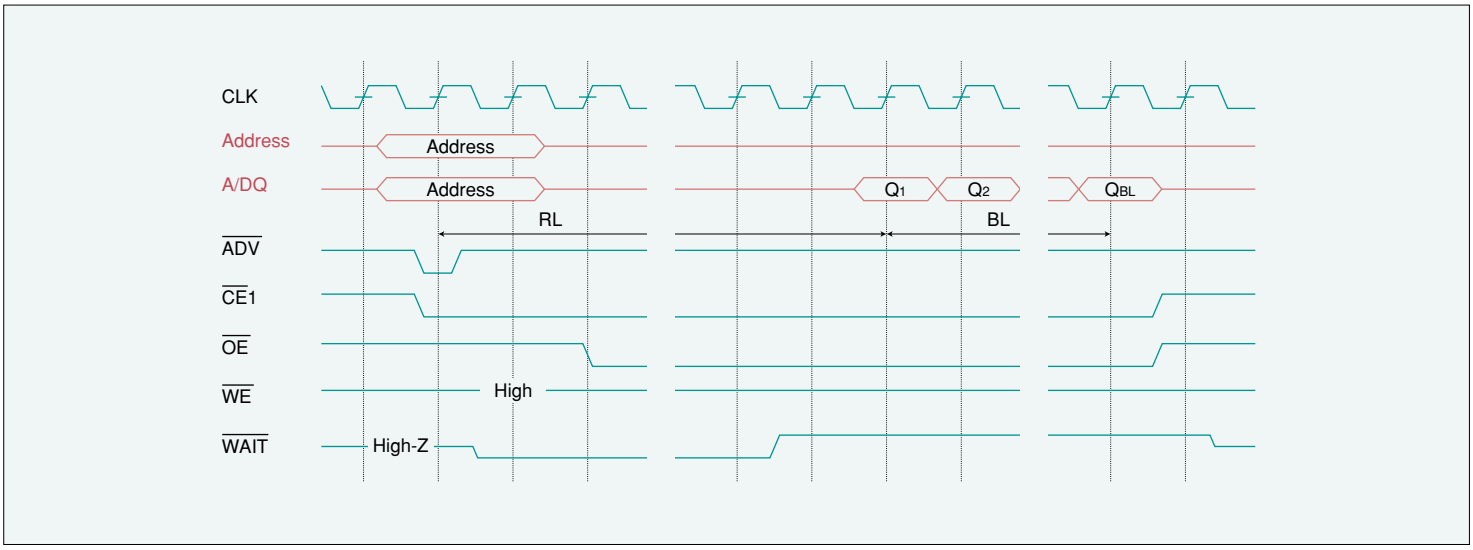
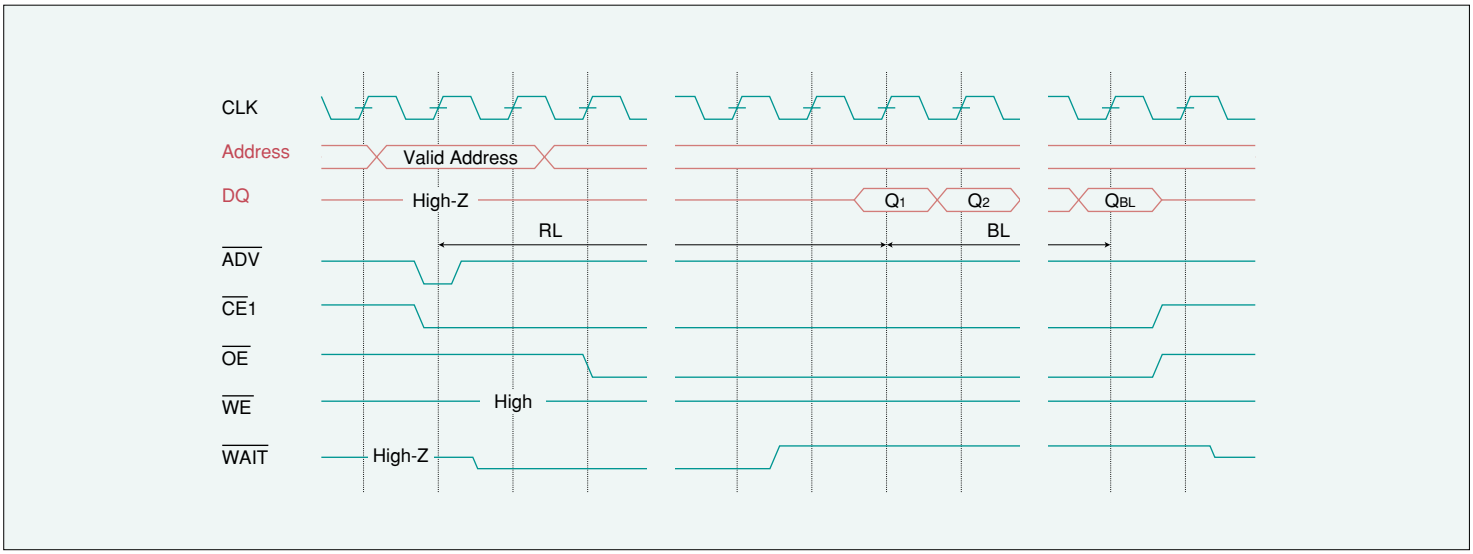


Figure 5 Read Timing for MB82DBS04164E



- I/O bus configuration: multiplexed address and data bus
- Power supply voltage: 1.7V to 1.95V
- Burst mode function (programmable burst length)
- Sleep mode and partial power-down mode
- Supply form: chip or wafer
  71-pin FBGA package (for samples only)

Conclusion

Fig.6 presents the development trends of Mobile FCRAM.

To meet market demand, FUJITSU has developed low- to large-density, high-speed and low-voltage products, as shown in Fig.6. These advanced products keep improving the functions like adopting DDR burst mode for high-speed performance and a multiplexed address and data bus configuration. Similar to large-density, low- and medium-density products are continuously improved features.

In addition to 128M-bit to 256M-bit products, FUJITSU has continued to support 16M-bit to 64M-bit Mobile FCRAM products to meet the demand for low- to medium-density. The revised products have more high-speed performance while maintaining low power consumption. Some medium-density products have a multiplexed address and data bus, helping reduce the design workload and cost.

MB82DBS02154E and MB82DBS04154E were designed to achieve that goal. While 32M-bit/64M-bit Mobile FCRAMs are already available, we believe that the products' reduced pin count will help save customers' total development costs.

FUJITSU will continue to develop FCRAM products to improve device performance and to offer our products as a total solution for improving customer design efficiency. ✱

NOTES

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Figure 6 Development Trends of Mobile FCRAM